University of Global Village (UGV), Barishal

Department of Electrical And Electronics Engineering

EEE 0714-2103
Electronics – 2

Course Content

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Electronics-II

Basic Course Information:

- **Course Title :** Electronics – 2
- **Course Code:** EEE 0714 – 2103
- **CIE Marks:** 90
- **SEE Marks:** 60
- **Exam Hours:** 2 hours (Mid term Examination)

  3 hours (Semester End Examination)
- **Semester:** 3rd Semester
- **Academic Session:** Winter 2025

Electronics-II

Assessment Pattern:

CIE – Continuous Internal Evaluation (90 Marks)

Bloom's Category Marks (out of 90)	Mid Term (45)	Assignment (15)	Quiz (15)	Attendance & External
Remember	05		05	
Understand	05	05	05	
Apply	10		05	15
Analyze	10			
Evaluate	10			
Create	05	05		

Electronics-II

Assessment Pattern:

SEE – Semester End Examination (60 Marks)

Bloom's Category Marks (out of 90)	Final Examination Term (60)
Remember	15
Understand	10
Apply	10
Analyze	10
Evaluate	10
Create	05

Course Learning Outcome (CLO's):

CLO1	Explain op amp structure. Describe the types of OPAMP
CLO2	Explain UJT structure and operation Will be able to explain OPAMP (operational amplifier) and its applications.
CLO3	Explain the gain of Op Amp applications
CLO4	Explains FET structure and operation. Translates the properties of n-channel and p- channel FET Calculates current and voltage of FET under the DC sources.
CLO5	Describes equivalent circuits of FET. Calculates current, voltage, and gain of FET under the Ac sources Will be able to explain the p-npn materials and devices.

Course Rationales:

This course introduces the advanced concepts of Electronics to the students. This course is required to understand and implement the advanced electronic circuits such as operational amplifiers, feedback amplifiers, frequency response, active filter etc. with the help of various problem solving.

Course Objectives

This course has been designed for the students.

1. To learn and understand the different applications of operational amplifiers, feedback amplifiers and power amplifier circuits.
2. Analyzing BJT and FET AC operation.
3. To design different electronic circuits.

Course Contents Summary

Sl. No.	Course Content	Hrs.	CLOs
1	Operational amplifiers (Op-Amp): Properties of ideal Op-Amps, non-inverting and inverting amplifiers, inverting integrators, differentiator, weighted summer, and other applications of Op-Amp circuits, effects of finite open loop gain and bandwidth on circuit performance, logic signal operation of Op-Amp, dc imperfections.	18	CLO1
2	Frequency response of amplifiers: Poles, zeros and Bode plots, amplifier transfer function, techniques of determining 3 dB frequencies of amplifier circuits, frequency response of single-stage and cascade amplifiers, frequency response of differential amplifiers.	12	CLO2
3	General purpose Op-Amp: DC analysis, small-signal analysis of different stages, gain and frequency response of 741 Op-Amp. Positive & Negative feedback: properties, basic topologies, and feedback amplifiers with different topologies, stability, and frequency compensation.	15	CLO3

Course Contents Summary

Sl. No.	Course Content	Hrs.	CLOs
4	Active filters: Different types of filters and specifications, transfer functions, realization of first and second order low, high and bandpass filters using Op-Amps.	9	CLO4
5	Signal generators: Basic principle of sinusoidal oscillation, Op-Amp RC oscillators, LC, and crystal oscillators, Hartly oscillators, colpitt oscillator's clapp oscillators. Power Amplifiers: Classification of output stages, class A, B and AB output stages.	6	CLO5

COURSE PLAN MAPPED WITH CLO

Week	Content of Course	Teaching-Learning Strategy	Assessment Strategy	Corresponding CLOs
1	Introduction to FET: Construction, operation, and characteristics of JFET.	Lecture, Visual Demonstration	Quiz, Problem Solving	CLO-1
2	Transfer Characteristics of FET: Analysis and practical examples.	Lecture, Practical Examples, Problem Solving	Problem Solving	CLO-1
3	MOSFET: Depletion and enhancement types, characteristics, and biasing techniques.	Lecture, Group Problem Solving, Demonstration	Assignment, Problem Solving	CLO-2
4	MOSFET Amplifier Design: Small signal model, analysis, and biasing for MOSFET amplifiers.	Lecture, Circuit Simulation	Quiz, Written Exam	CLO-2

COURSE PLAN MAPPED WITH CLO

Week	Course Content	Teaching-Learning Strategy	Assessment Strategy	Corresponding CLOs
5	CMOS and VMOS Devices: Characteristics, design considerations, and VVR applications.	Lecture, Design Activities	Problem Solving, Assignment	CLO-2
6	FET Small Signal Model: Equivalent circuits, voltage gain, and frequency response analysis.	Lecture, Practical Demonstration	Assignment	CLO-2
7	Class Test-1	Review, Problem Solving	Class Test	CLO-1, CLO-2
8	Power Amplifiers: Introduction, Untuned Class A and AB amplifiers.	Lecture, Case Studies	Problem Solving	CLO-3,4
9	Power Amplifiers: Class B and Class C amplifiers, push-pull configurations.	Lecture, Practical Examples, Design Analysis	Quiz, Problem Solving	CLO-4,5

COURSE PLAN MAPPED WITH CLO

Week	Course Content	Teaching-Learning Strategy	Assessment Strategy	Corresponding CLOs
10	Tuned Power Amplifiers: Single and double-tuned cascaded amplifiers.	Lecture, Circuit Simulations	Problem Solving, Assignment	CLO-3
11	Neutralization Techniques: Applications of feedback to improve amplifier stability.	Lecture, Case Studies, Problem Solving	Problem Solving, Written Exam	CLO-3,5
12	Class Test-2	Review, Problem Solving	Class Test	CLO-2, CLO-3,4
13	Operational Amplifiers (P-AMP): Types, characteristics, and configurations.	Lecture, Group Activities	Quiz, Problem Solving	CLO-4,5
14	Op-Amp Applications: Differentiators, integrators, and comparator circuits.	Lecture, Design Activities	Assignment, Problem Solving	CLO-4,5

COURSE PLAN MAPPED WITH CLO

Week	Course Content	Teaching-Learning Strategy	Assessment Strategy	Corresponding CLOs
15	Analog Computers: Applications in solving differential equations using active filters.	Lecture, Simulation, Design Tasks	Written Exam	CLO-5
16	Active Filters: Low-pass, high-pass, and band-pass filter design using Op-Amps.	Lecture, Practical Examples	Problem Solving	CLO-4,5
17	Viva and Presentation: Comprehensive evaluation on FET, MOSFET, Power Amplifiers, and Op-Amps.	Viva-Voce, Student Presentations	Viva, Presentation	CLO-1, CLO-2, CLO-3, CLO-4, CLO-5

Reference Books

- Electronic Devices and Circuit Theory by R. Boylestad
- Other Electronics Book

Learning Outcome:

- Student will learn about the basic theory of FET, OP-AMP, and power amplifier. They will be able to design different electronic circuits based on FET, OP-AMP, and power amplifier

Teaching Methodology/Strategy

- 1. Power point presentation, 2. White board 3. Question-answer in the class, 4. Student's presentation, 5. Assignment

Week - 1

FETs vs. BJTs

FET>>Field Effect Transistor
BJT>>Bipolar Junction Transistor
Similarities:

- **Amplifiers**
- **Switching devices**
- **Impedance matching circuits**

Few Differences:

- **FETs are voltage-controlled devices. BJTs are current controlled devices.**
- **FETs have a higher input impedance. BJTs have higher gains.**
- **FETs are less sensitive to temperature variations and are more easily integrated on ICs.**
- **FETs are generally more static sensitive than BJTs.**

FET Types

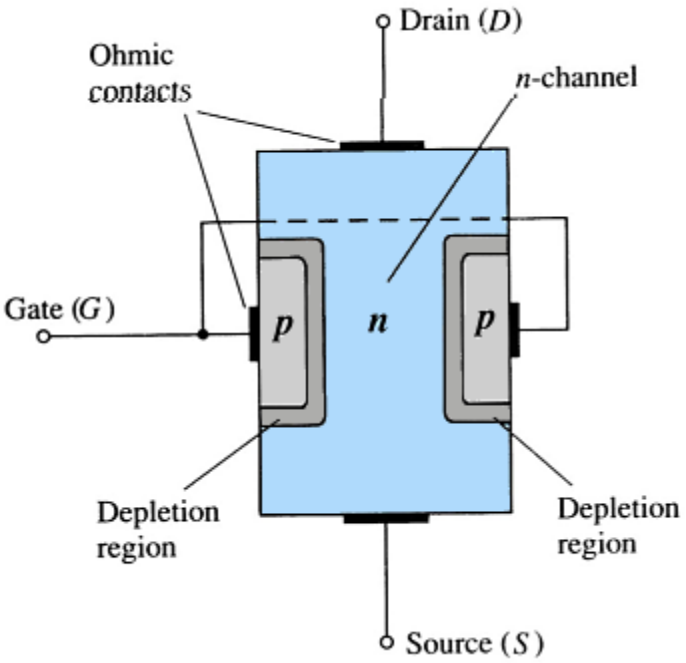
- **JFET:** **Junction FET**
- **MOSFET:** **Metal–Oxide–Semiconductor FET**
  - **D-MOSFET:** **Depletion MOSFET**
  - **E-MOSFET:** **Enhancement MOSFET**

JFET Construction

There are two types of JFETs

- ***n*-channel**
- ***p*-channel**

The n-channel is more widely used.



There are three terminals:

- **Drain (D) and Source (S) are connected to the *n*-channel**
- **Gate (G) is connected to the *p*-type material**

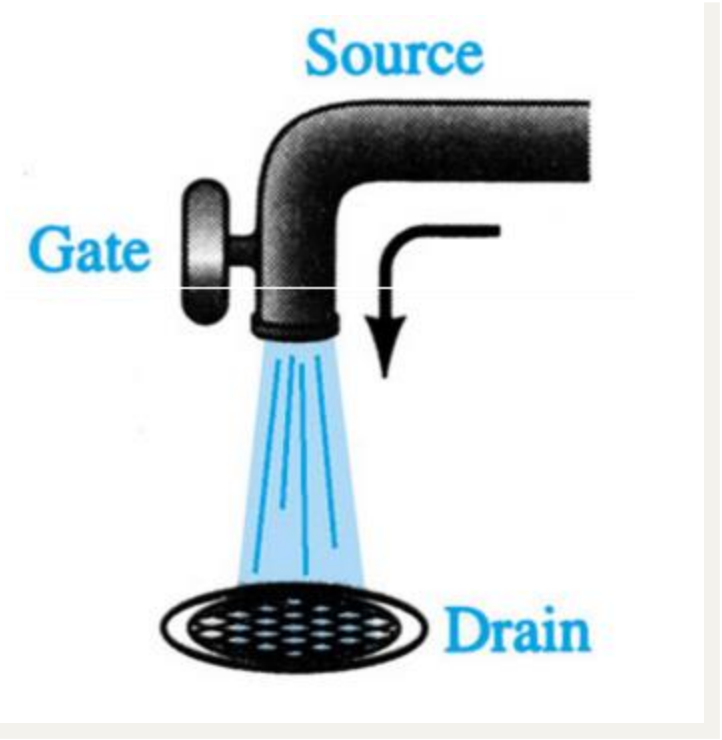
JFET Operation: The Basic Idea

JFET operation can be compared to a water spigot.

The source of water pressure is the accumulation of electrons at the negative pole of the drain-source voltage.

The drain of water is the electron deficiency (or holes) at the positive pole of the applied voltage.

The control of flow of water is the gate voltage that controls the width of the n-channel and, therefore, the flow of charges from source to drain.



JFET Operating Characteristics

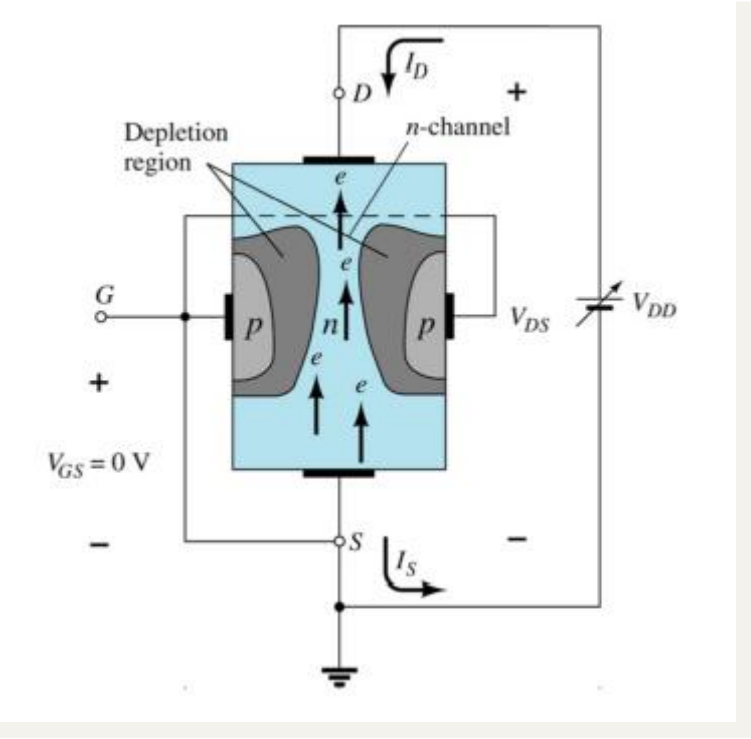
There are three basic operating conditions for a JFET:

- **V_{GS} = 0, V_{DS} increasing to some positive value**
- **V_{GS} < 0, V_{DS} at some positive value**
- **Voltage-controlled resistor**

JFET Operating Characteristics: $V_{GS} = 0V$

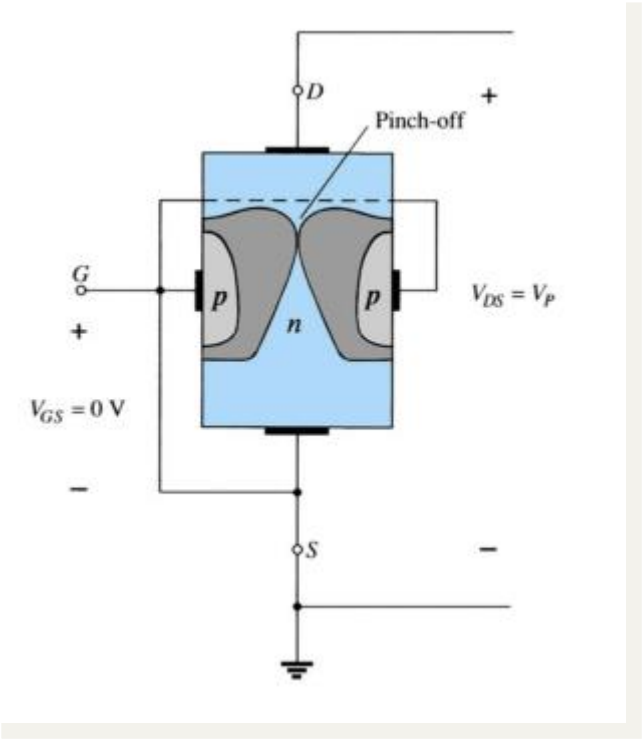
Three things happen when $V_{GS} = 0$ and V_{DS} is increased from 0 to a more positive voltage

- **The depletion region between p-gate and n-channel increases as electrons from n-channel combine with holes from p-gate.**
- **Increasing the depletion region, decreases the size of the n-channel which increases the resistance of the n-channel.**
- **Even though the n-channel resistance is increasing, the current (I_D) from source to drain through the n-channel is increasing. This is because V_{DS} is increasing.**



If V_{GS} = 0 and V_{DS} is further increased to a more positive voltage, then the depletion zone gets so large that it pinches off the n-channel.

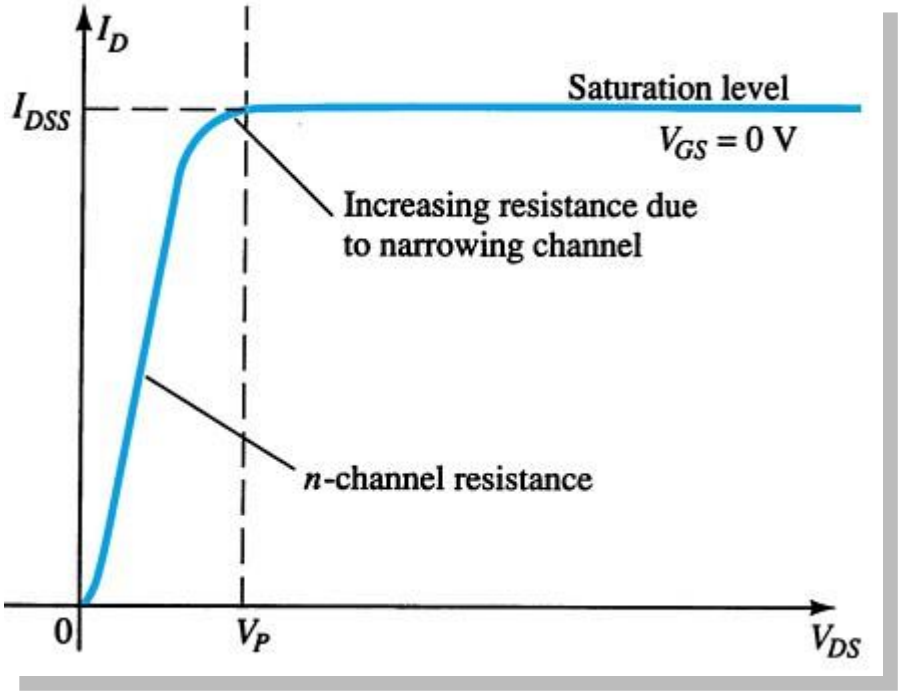
This suggests that the current in the n-channel (I_D) would drop to 0A, but it does just the opposite–as V_{DS} increases, so does I_D.



JFET Operating Characteristics: Saturation

At the pinch-off point:

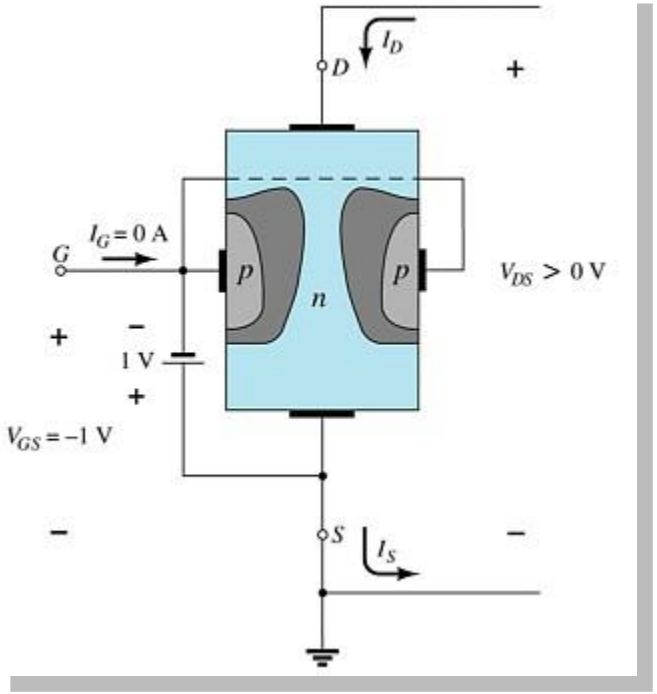
- **Any further increase in V_{GS} does not produce any increase in I_D. V_{GS} at pinch-off is denoted as V_p.**
- **I_D is at saturation or maximum. It is referred to as I_{DSS}.**
- **The ohmic value of the channel is maximum.**



Week - 2

JFET Operating Characteristics

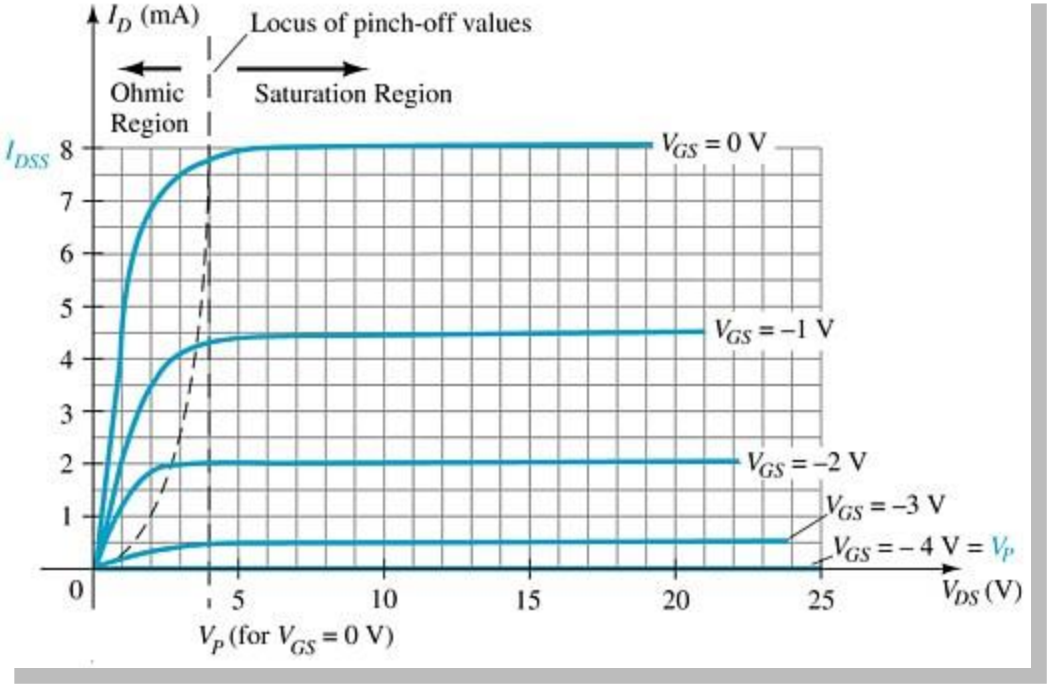
As V_{GS} becomes more negative, the depletion region increases.



JFET Operating Characteristics

As V_{GS} becomes more negative:

- **The JFET experiences pinch-off at a lower voltage (V_P).**
- **I_D decreases ($I_D < I_{DSS}$) even though V_{DS} is increased.**
- **Eventually I_D reaches 0 A. V_{GS} at this point is called V_p or $V_{GS(off)}$..**

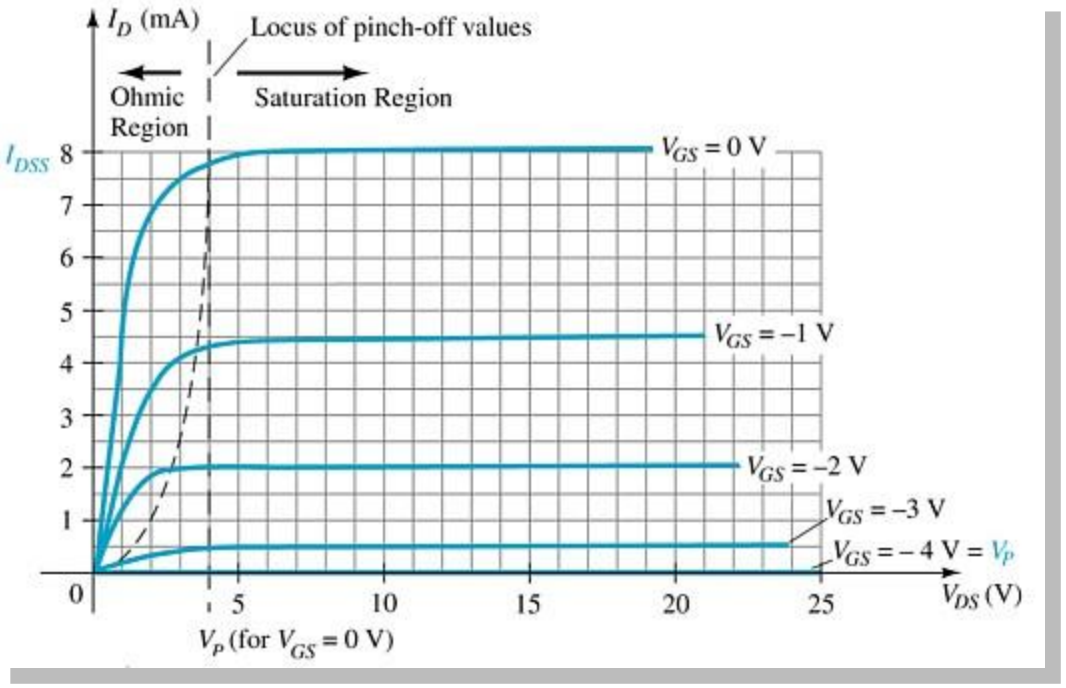


Also note that at high levels of V_{DS} the JFET reaches a breakdown situation. I_D increases uncontrollably if $V_{DS} > V_{DSmax}$.

The region to the left of the pinch-off point is called the ohmic region.

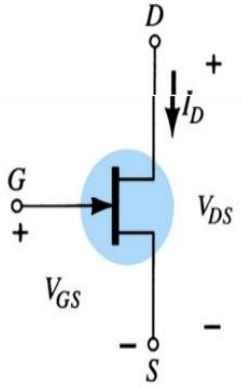
The JFET can be used as a variable resistor, where V_{GS} controls the drain-source resistance (r_d). As V_{GS} becomes more negative, the resistance (r_d) increases.

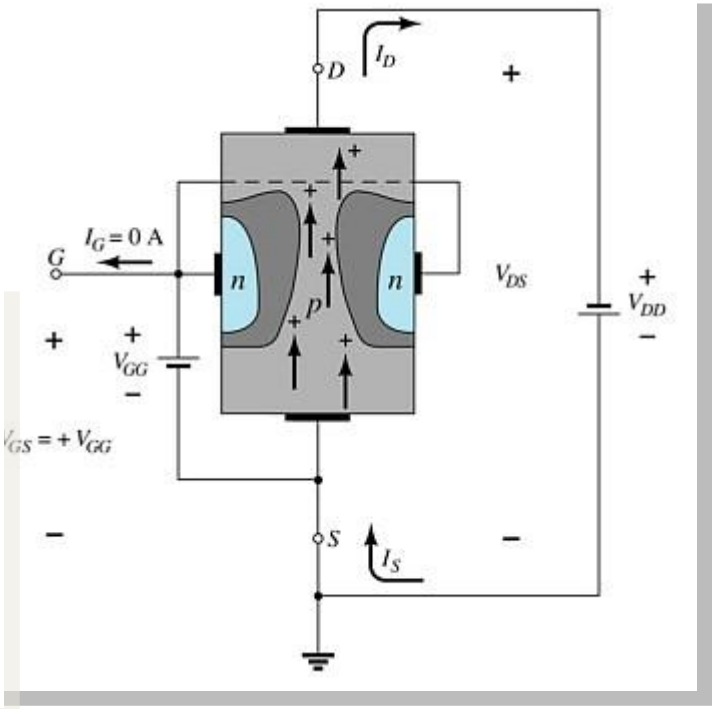
$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$



p-Channel JFETS

The *p*-channel JFET behaves the same as the *n*-channel JFET, except the voltage polarities and current directions are reversed.

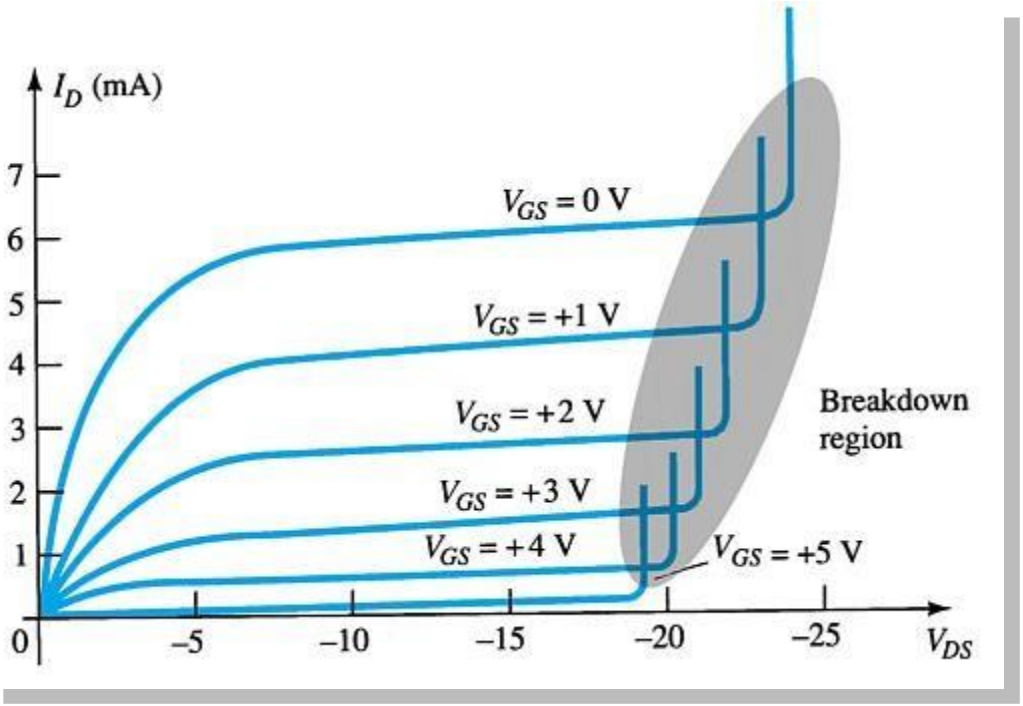




p-Channel JFET Characteristics

As V_{GS} increases more positively

- **The depletion zone increases**
- **I_D decreases ($I_D < I_{DSS}$)**
- **Eventually $I_D = 0$ A**



Also note that at high levels of V_{DS} the JFET reaches a breakdown situation: I_D increases uncontrollably if $V_{DS} > V_{DSmax}$.

JFET Transfer Characteristics

The transfer characteristic of input-to-output is not as straightforward in a JFET as it is in a BJT.

In a BJT, β indicates the relationship between I_B (input) and I_C (output).

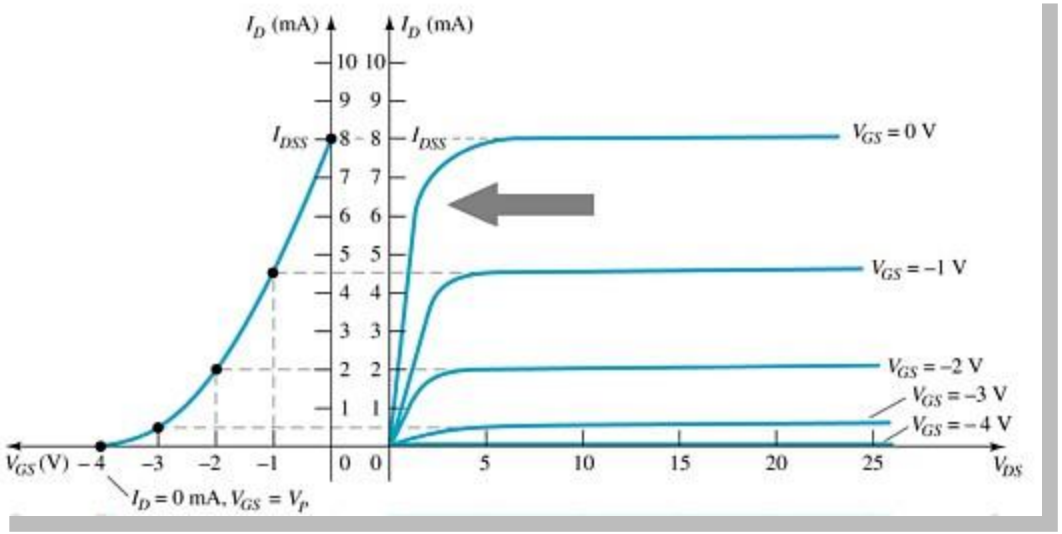
In a JFET, the relationship of V_{GS} (input) and I_D (output) is a little more complicated:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Shockley's Equation

JFET Transfer Curve

This graph shows the value of I_D for a given value of V_{GS}.



Plotting the JFET Transfer Curve

Using I_{DSS} and Vp ($V_{GS(off)}$) values found in a specification sheet, the transfer curve can be plotted according to these three steps:

Step 1

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Solving for V_{GS} = 0V $I_D = I_{DSS}$

Step 2

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Solving for $V_{GS} = V_p$ ($V_{GS(off)}$) $I_D = 0A$

Step 3

Solving for V_{GS} = 0V to V_p $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

Week - 3

MOSFETs

MOSFETs have characteristics similar to JFETs and additional characteristics that make then very useful.

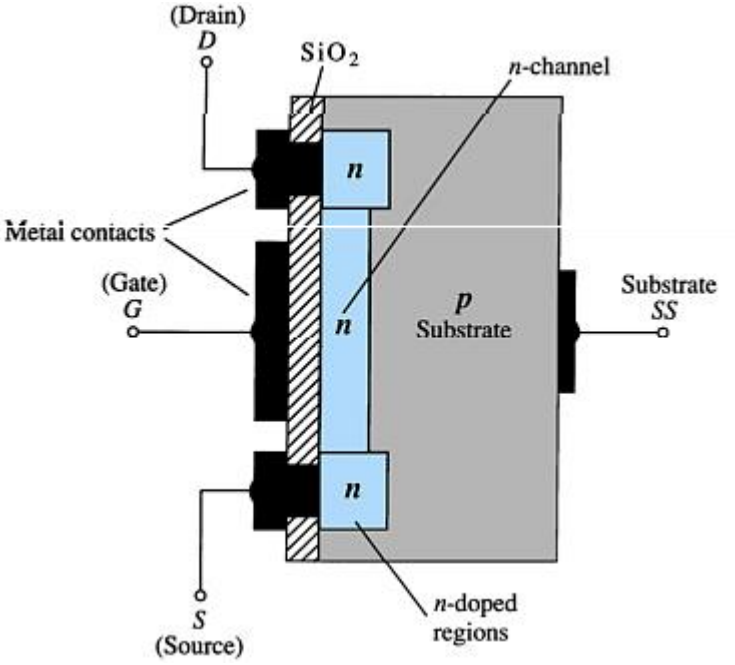
There are two types of MOSFETs:

- **Depletion-Type**
- **Enhancement-Type**

Depletion-Type MOSFET Construction

The Drain (D) and Source (S) connect to the to *n*-doped regions. These *n*-doped regions are connected via an *n*-channel. This *n*-channel is connected to the Gate (G) via a thin insulating layer of SiO_2.

The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called Substrate (SS).



Basic Operation and Characteristics

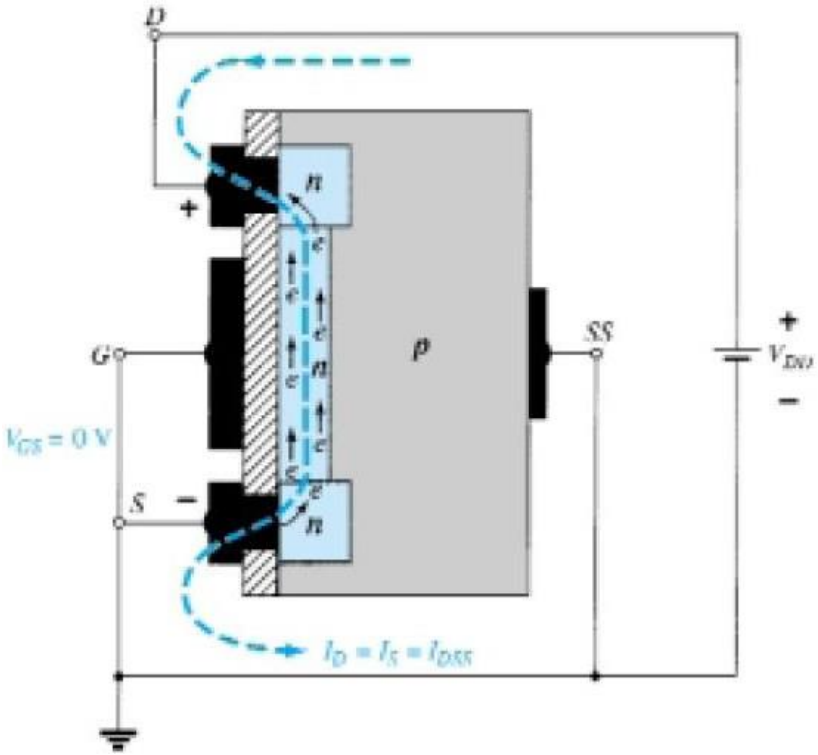


Figure 5.24 *n*-Channel depletion-type MOSFET with $V_{GS} = 0$ V and an applied voltage V_{DD}.

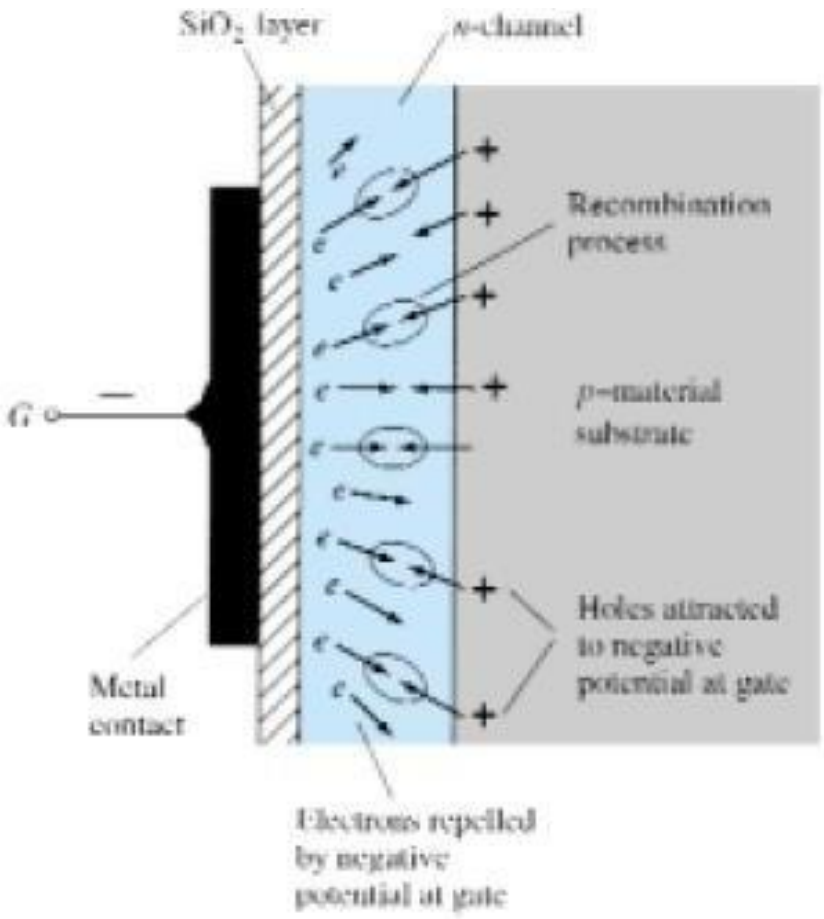


Figure 5.26 Reduction in free carriers in channel due to a negative potential at the gate terminal.

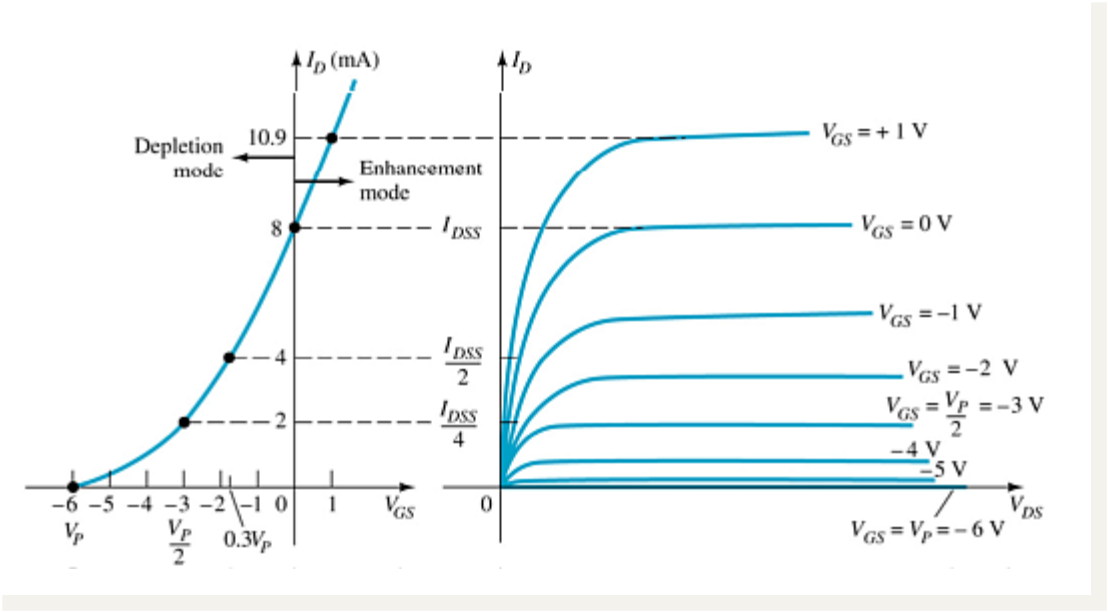
Applying negative voltage at gate

Applying positive voltage at gate?? What will happen

Basic MOSFET Operation

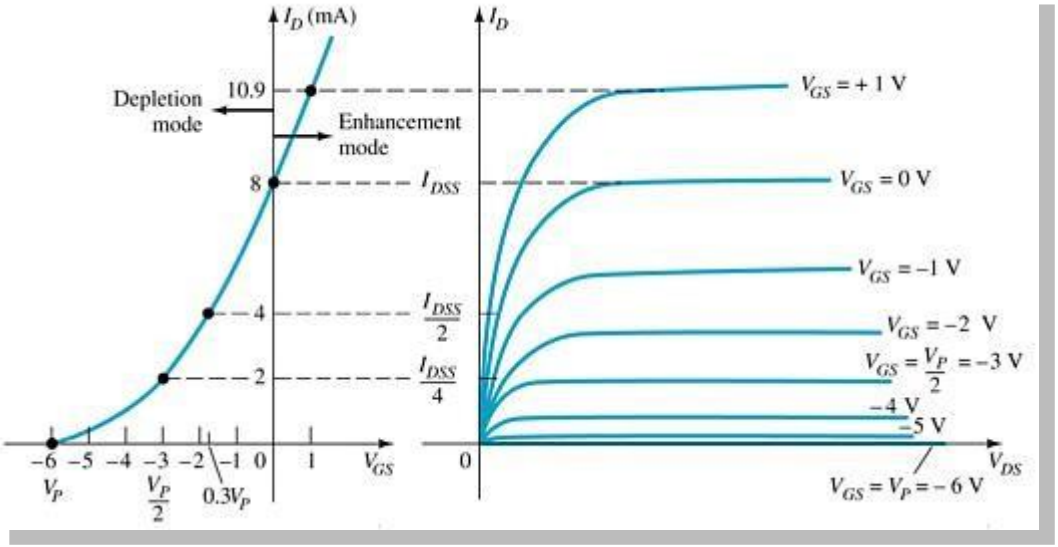
A depletion-type MOSFET can operate in two modes:

- **Depletion mode**
- **Enhancement mode**



D-Type MOSFET in Depletion Mode

Depletion Mode



The characteristics are similar to a JFET.

- **When $V_{GS} = 0$ V, $I_D = I_{DSS}$**
- **When $V_{GS} < 0$ V, $I_D < I_{DSS}$**
- **The formula used to plot the transfer curve still applies:**

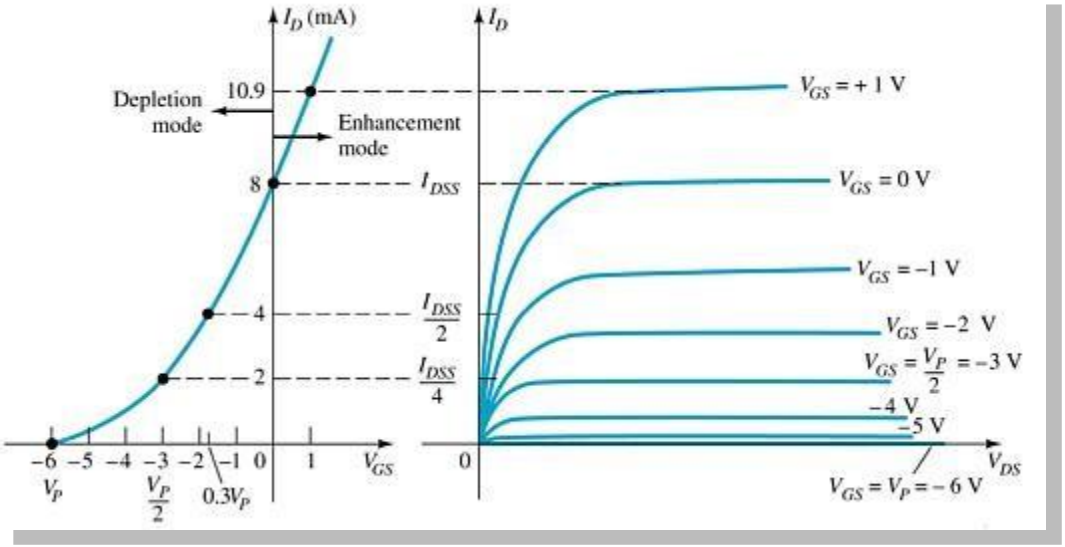
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

D-Type MOSFET in Enhancement Mode

Enhancement Mode

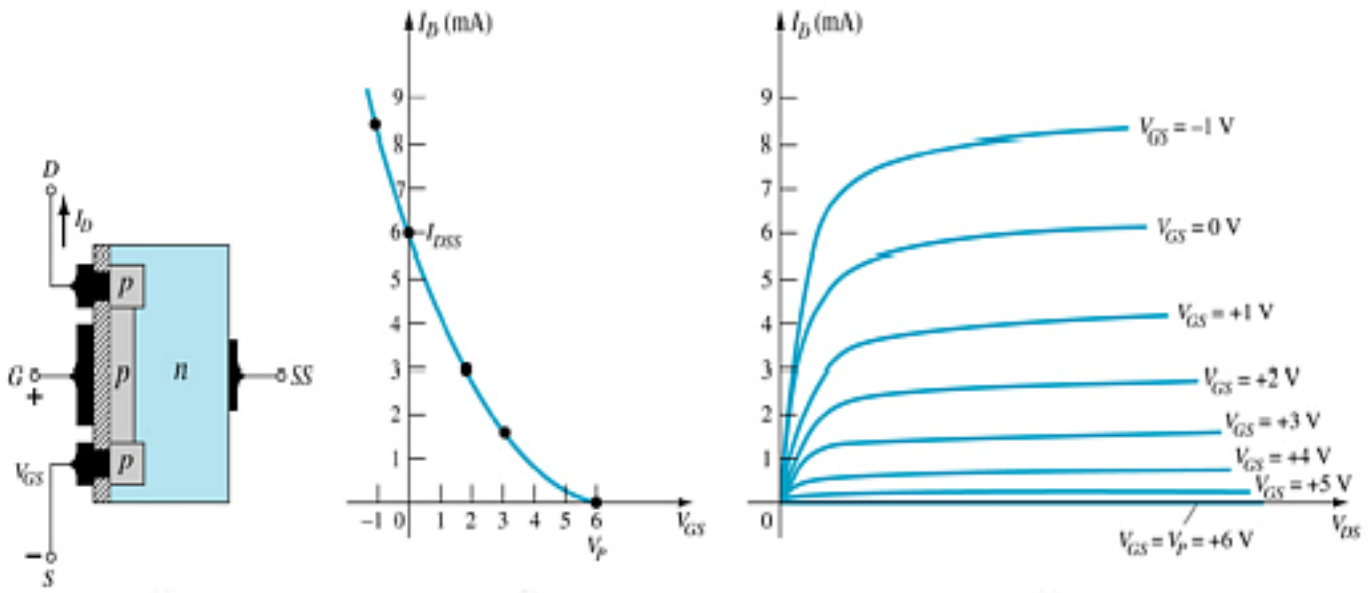
- $V_{GS} > 0$ V
- I_D increases above I_{DSS}
- The formula used to plot the transfer curve still applies:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

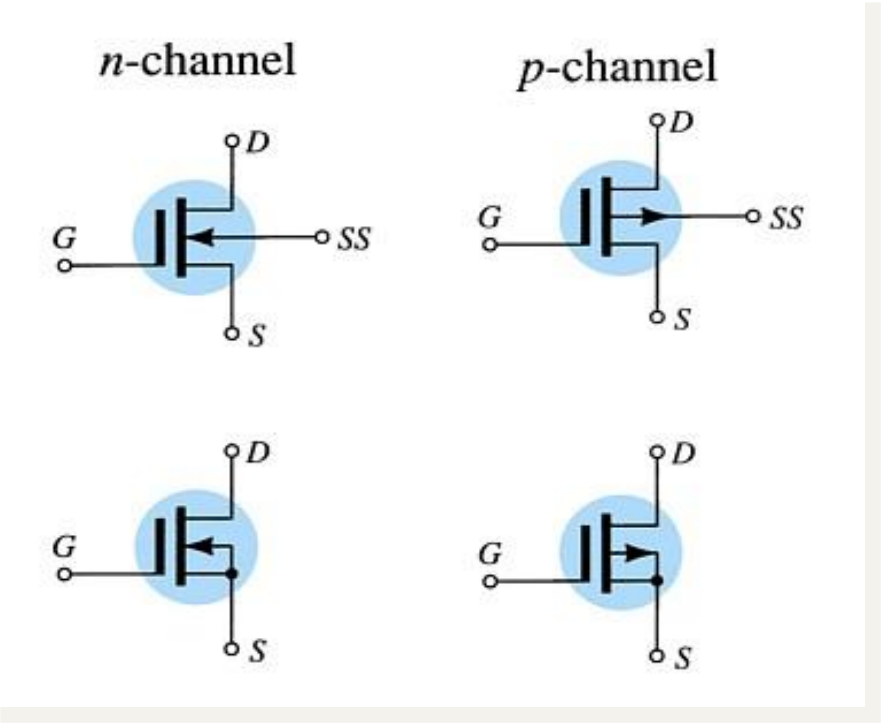


Note that V_{GS} is now a positive polarity

p-Channel D-Type MOSFET



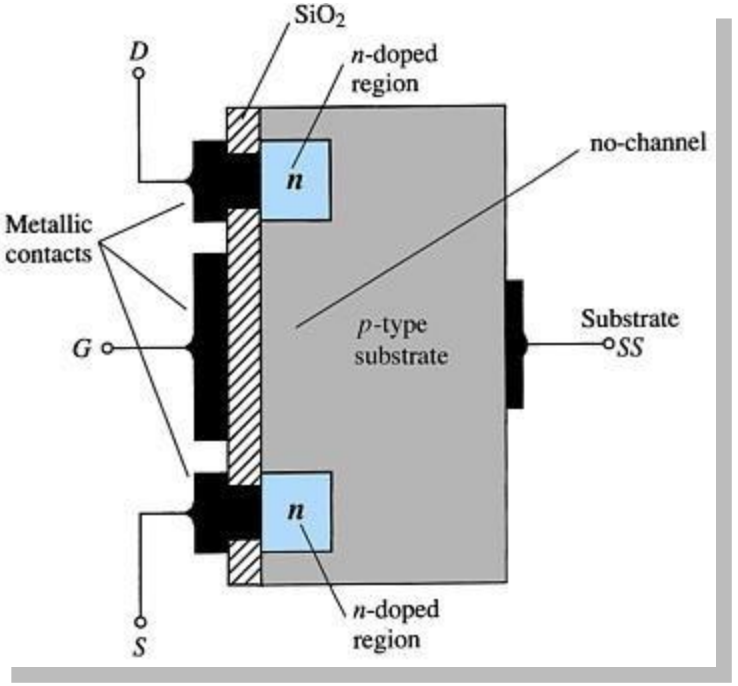
D-Type MOSFET Symbols



Week - 4

E-Type MOSFET Construction

- The **Drain** (D) and **Source** (S) connect to the to *n*-doped regions. These *n*-doped regions are connected via an *n*-channel
- The **Gate** (G) connects to the *p*-doped substrate via a thin insulating layer of SiO_2
- There is no channel
- The *n*-doped material lies on a *p*-doped substrate that may have an additional terminal connection called the **Substrate** (SS)



Channel Formation

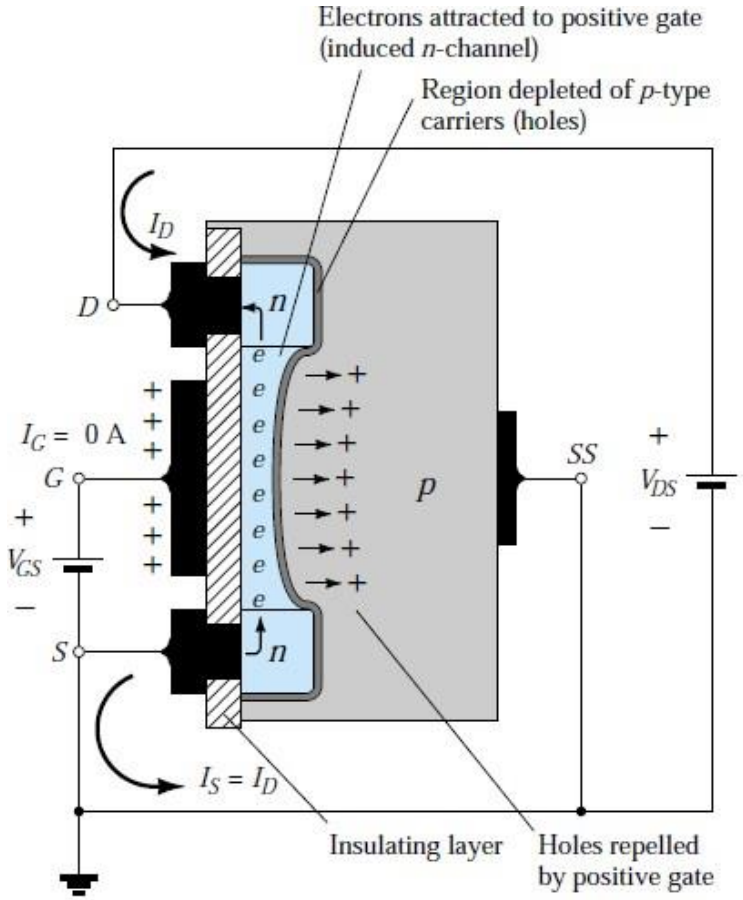


Figure 5.32 Channel formation in the *n*-channel enhancement-type MOSFET.

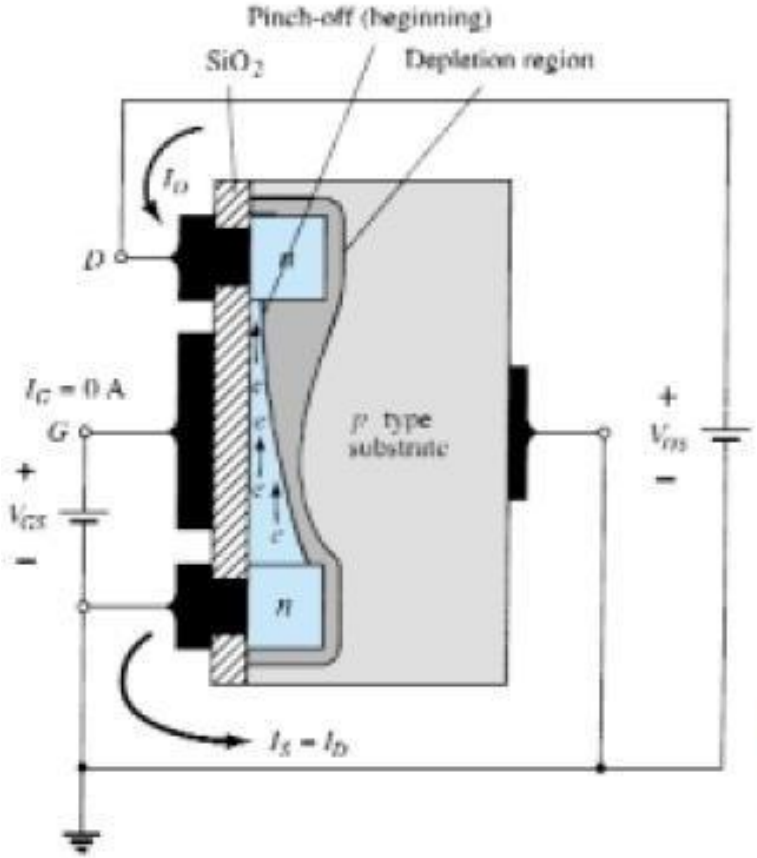
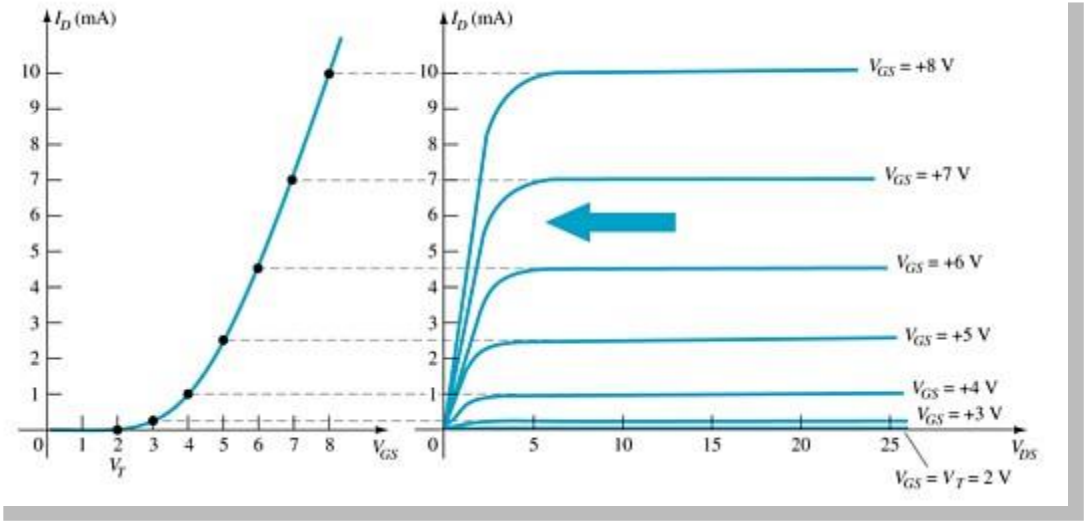


Figure 5.33 Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS}.

Basic Operation of the E-Type MOSFET

The enhancement-type MOSFET operates only in the enhancement mode.

- **V_{GS} is always positive**
- **As V_{GS} increases, I_D increases**
- **As V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS}) and the saturation level, V_{DSsat} is reached**



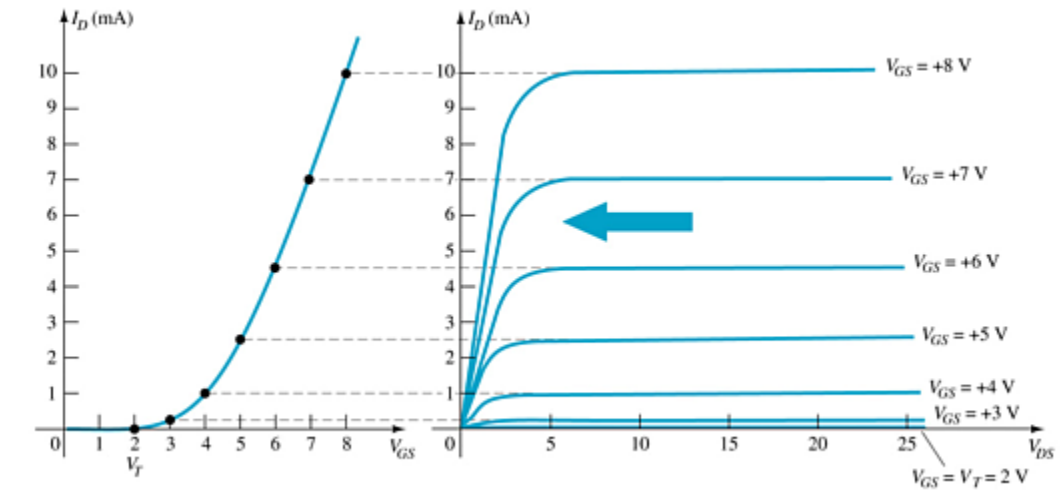
E-Type MOSFET Transfer Curve

To determine I_D given V_{GS}:

$$I_D = k(V_{GS} - V_T)^2$$

Where:

V_T = threshold voltage or voltage at which the MOSFET turns on



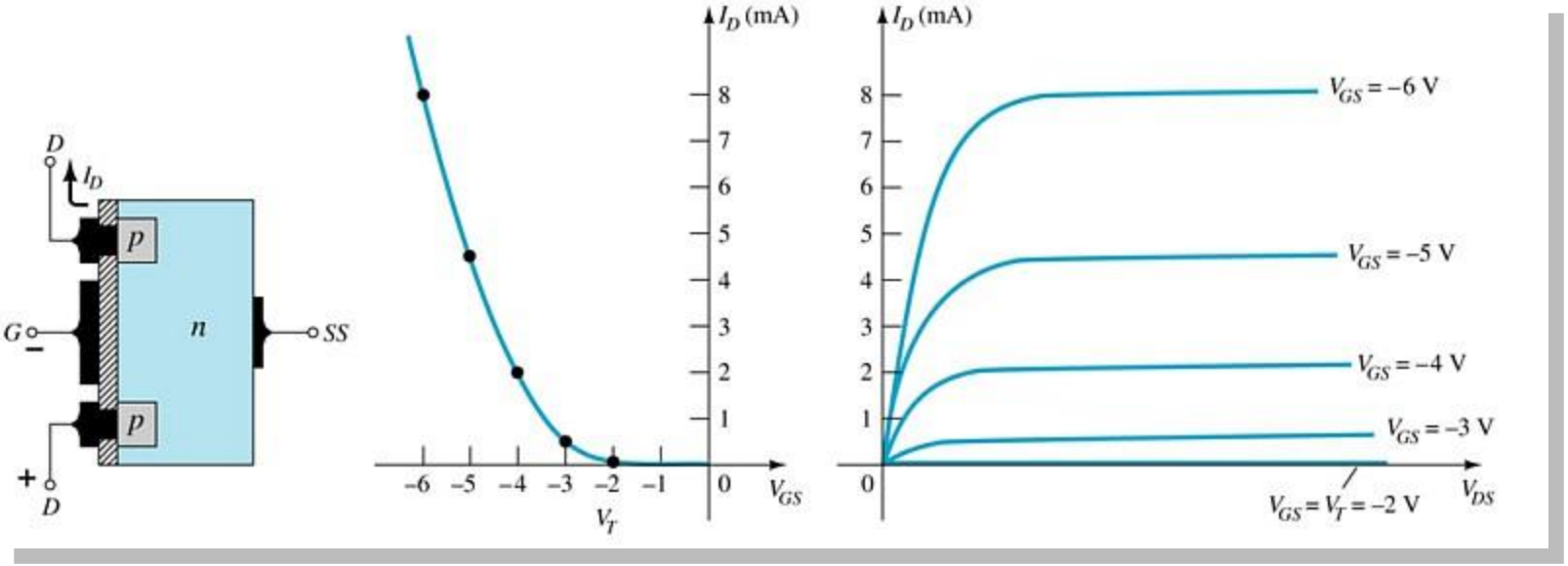
***k*, a constant, can be determined by using values at a specific point and the formula:**

$$k = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$

V_{DSsat} can be calculated by:

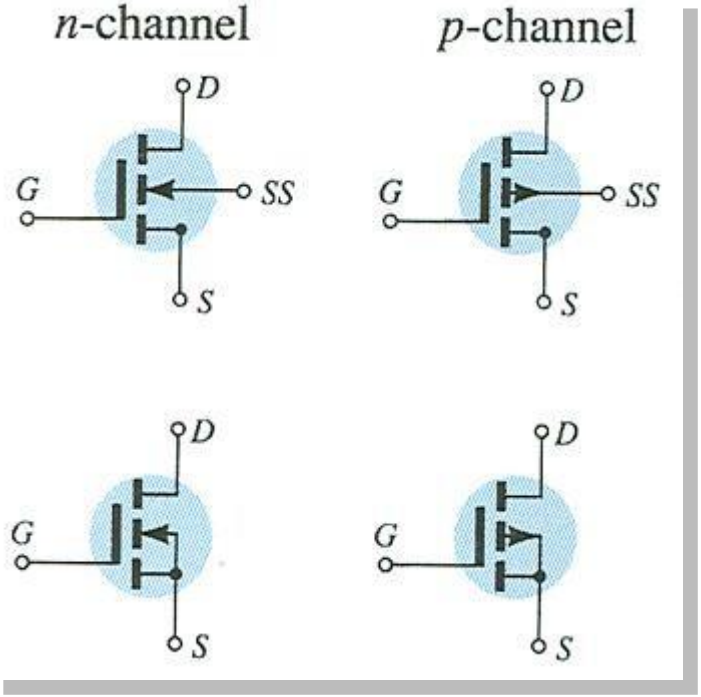
$$V_{Dsat} = V_{GS} - V_T$$

p-Channel E-Type MOSFETs



The *p*-channel enhancement-type MOSFET is similar to the *n*-channel, except that the voltage polarities and current directions are reversed.

MOSFET Symbols



Handling MOSFETs

MOSFETs are very sensitive to static electricity. Because of the very thin SiO_2 layer between the external terminals and the layers of the device, any small electrical discharge can create an unwanted conduction.

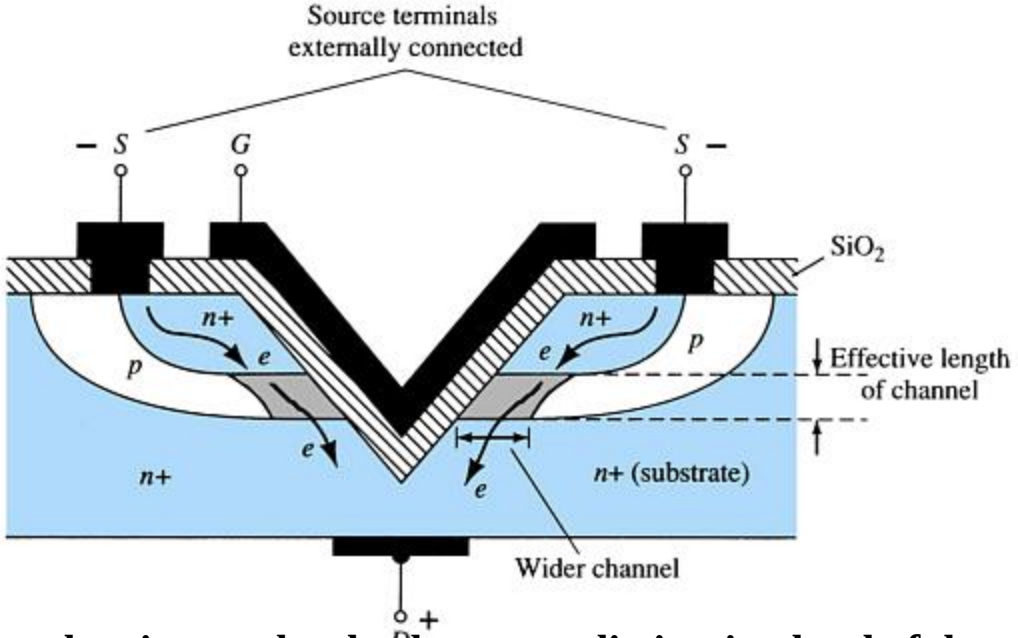
Protection

- **Always transport in a static sensitive bag**
- **Always wear a static strap when handling MOSFETS**
-
- **Apply voltage limiting devices between the gate and source, such as back-to-back Zeners to limit any transient voltage.**

VMOS Devices

VMOS (vertical MOSFET) increases the surface area of the device.

One of the disadvantages of the typical MOSFET is the reduced power-handling levels (typically, less than 1 W) compared to BJT transistors.

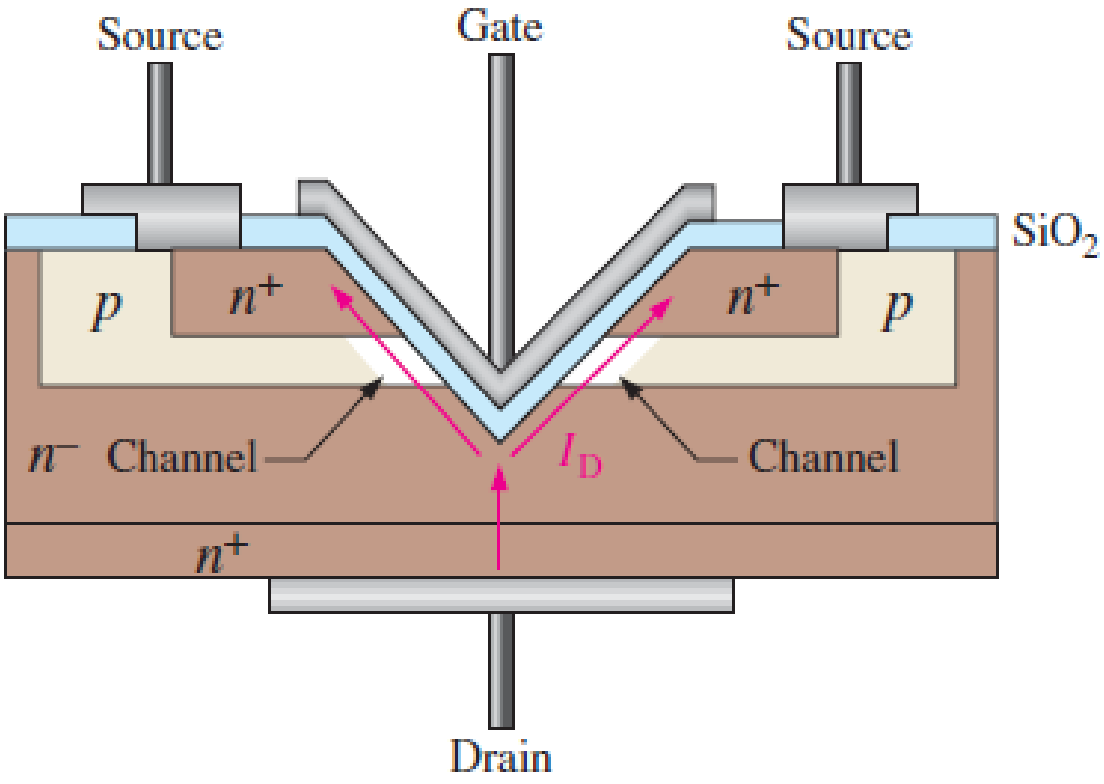


Advantages

- **VMOS devices handle higher currents by providing more surface area to dissipate the heat.**
- **VMOS devices also have faster switching times.**
- **VMOS FETs have a positive temperature coefficient that will combat the possibility of thermal runaway**

decreasing channel lengths result in reduced resistance levels, the power dissipation level of the device (power lost in the form of heat) at operating current levels will be reduced. In addition, the contact area between the channel and the *n* region is greatly increased by the vertical mode construction, contributing to a further decrease in the resistance level and an increased area for current between the doping layers

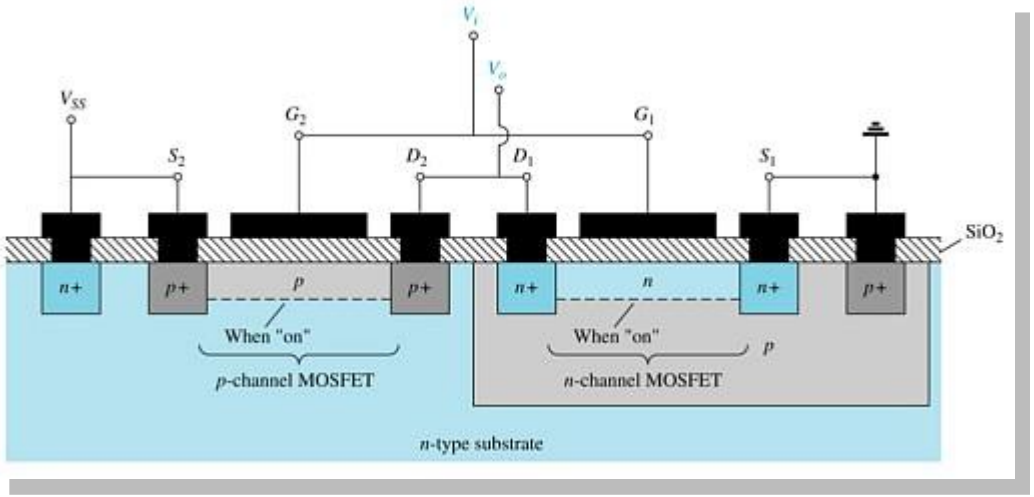
n^+ substrate where n^+ means a higher doping level than n^-



Week - 5

CMOS Devices

CMOS (complementary MOSFET) uses a *p*-channel and *n*-channel MOSFET; often on the same substrate as shown here.

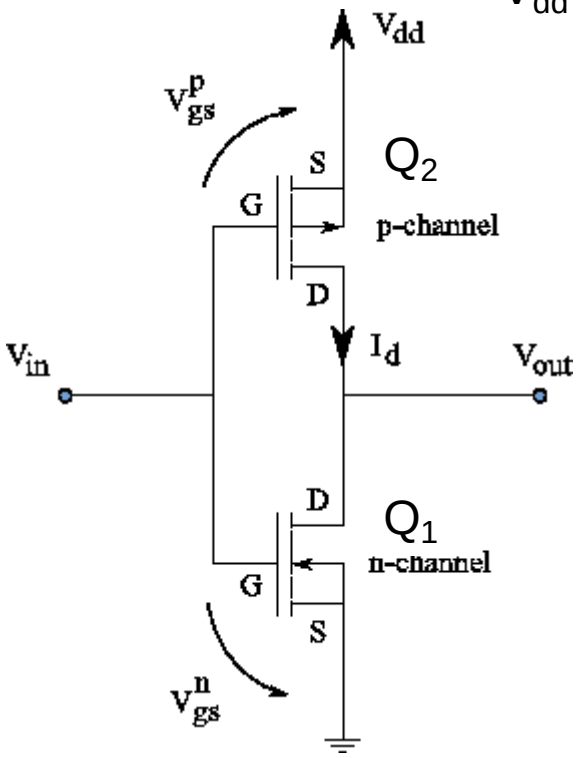


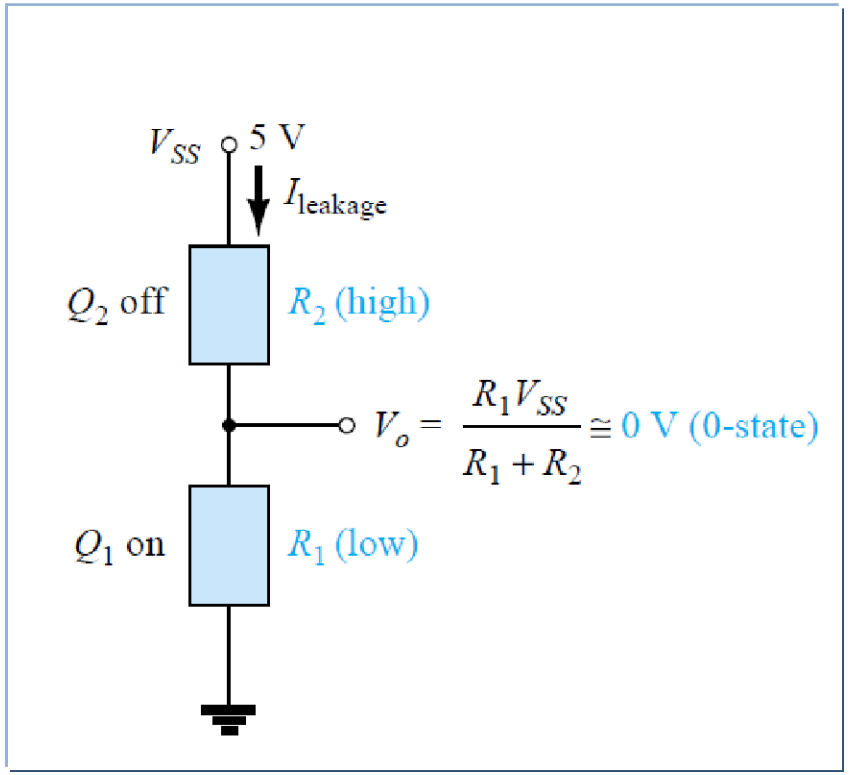
Advantages

- **Useful in logic circuit designs**
- **Higher input impedance**
- **Faster switching speeds**
- **Lower operating power levels**

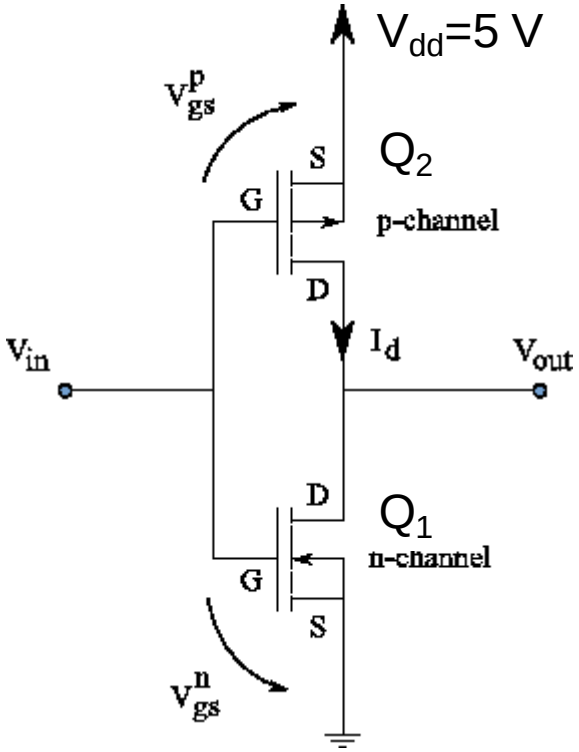
CMOC Inverter

V_{dd}=5 V





CMOC Inverter: Operation



V_{in}	$V_{gs(n)}$	$V_{gs(p)}$	Q_1	Q_2	V_{out}	
5 V	+5	0	On/short	Off/open	0	
0 V	0	-5	Off/open	On/short	5	

Common FET Biasing Circuits

JFET Biasing Circuits

- **Fixed – Bias**
- **Self-Bias**
- **Voltage-Divider Bias**

D-Type MOSFET Biasing Circuits

- **Self-Bias**
- **Voltage-Divider Bias**

E-Type MOSFET Biasing Circuits

- **Feedback Configuration**
- **Voltage-Divider Bias**

For all FETs:

$$I_G \cong 0A$$

$$I_D = I_S$$

For JFETS and D-Type MOSFETs:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

For E-Type MOSFETs:

$$I_D = k(V_{GS} - V_T)^2$$

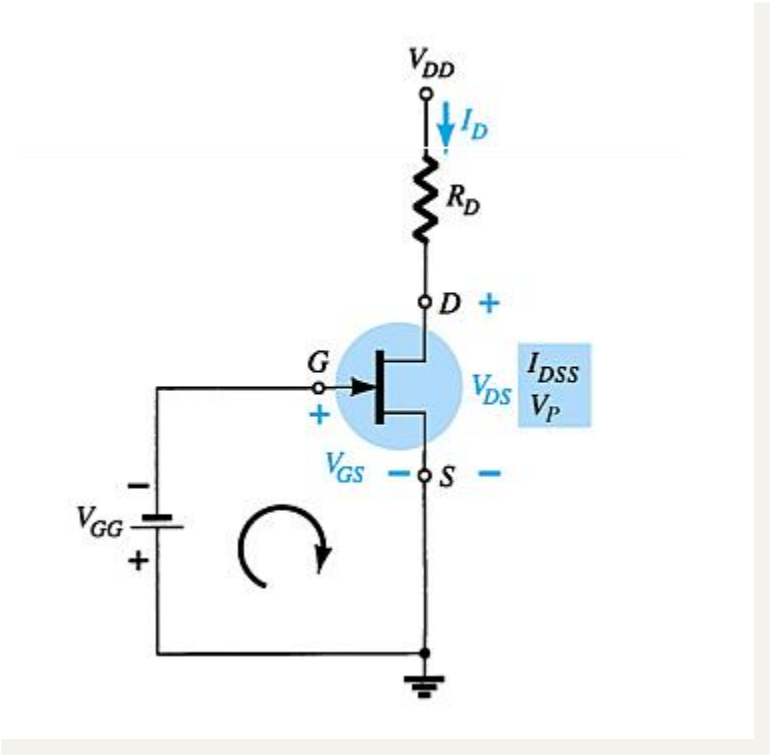
$$V_{DS} = V_{DD} - I_D R_D$$

$$V_S = 0V$$

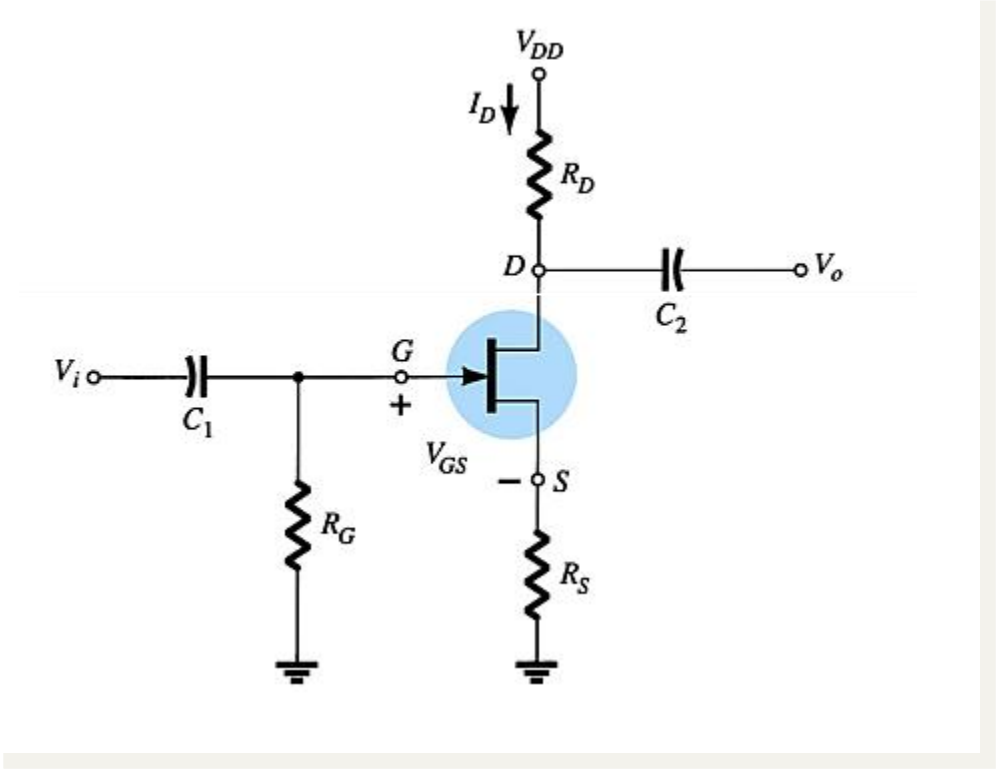
$$V_C = V_{DS}$$

$$V = V_{GS}$$

$$V_{GS} = -V_{GG}$$



Self-Bias Configuration



For the indicated loop, $V_{GS} = -I_D R_S$

To solve this equation:

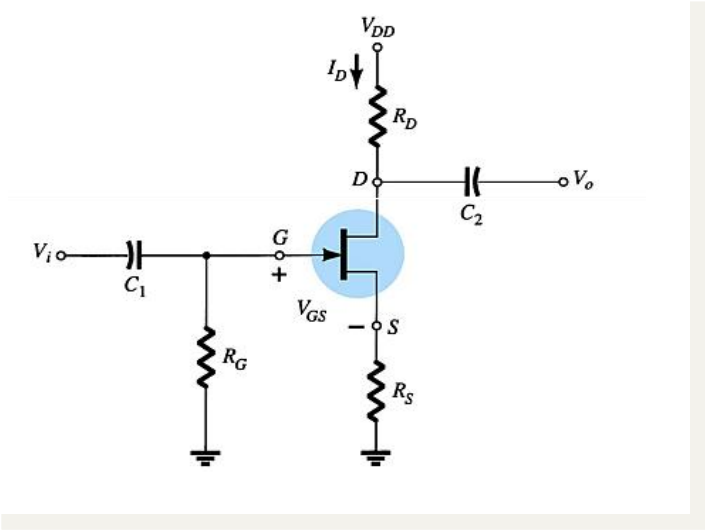
- **Select an $I_D < I_{DSS}$ and use the component value of R_S to calculate V_{GS}**
- **Plot the point identified by I_D and V_{GS}. Draw a line from the origin of the axis to this point.**
- **Plot the transfer curve using I_{DSS} and V_P ($V_P = V_{GSoff}$ in specification sheets) and a few points such as $I_D = I_{DSS}/4$ and $I_D = I_{DSS}/2$ etc.**

The Q-point is located where the first line intersects the transfer curve. Use the value of I_D at the Q-point (I_{DQ}) to solve for the other voltages:

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

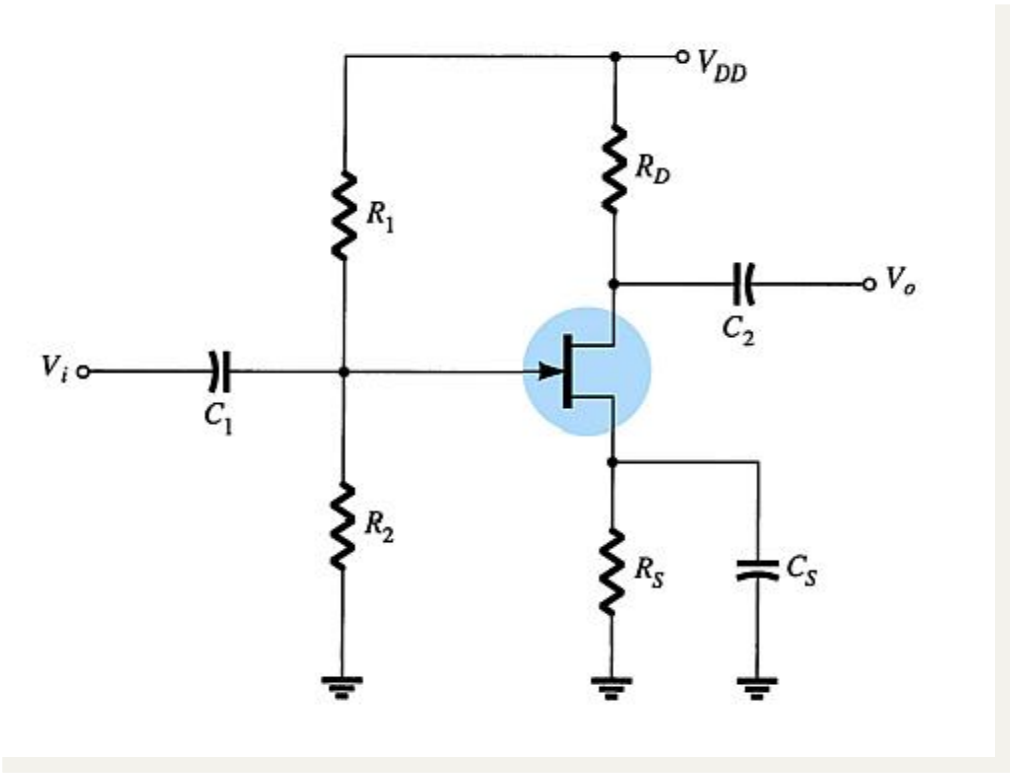
$$V_S = I_D R_S$$

$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$



$I_G = 0$ A

I_D responds to changes in V_{GS}.



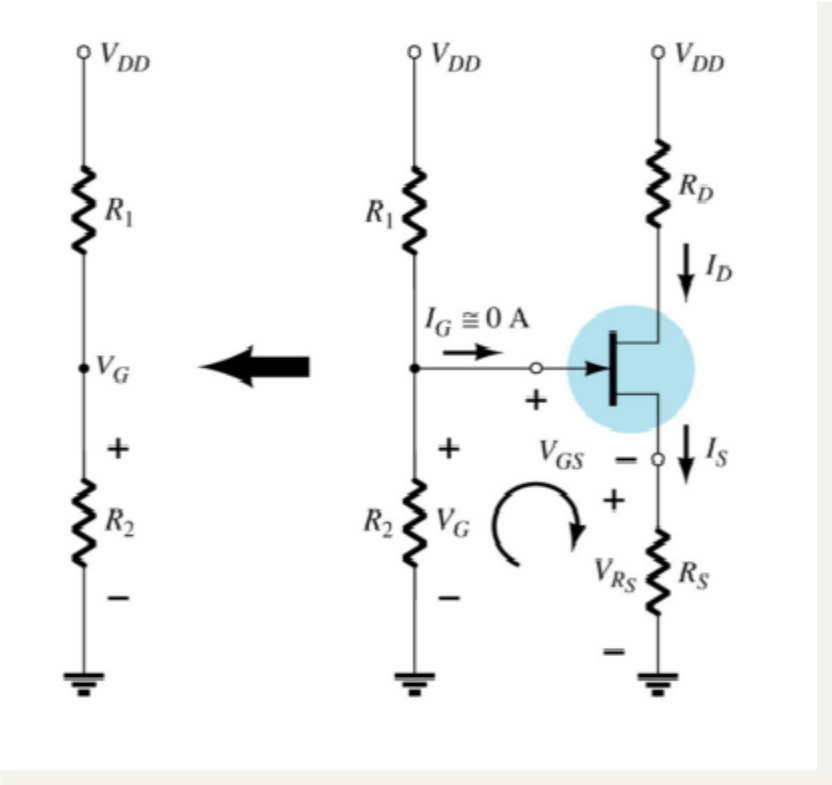
V_G is equal to the voltage across divider resistor R_2:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Using Kirchhoff's Law:

$$V_{GS} = V_G - I_D R_S$$

The Q point is established by plotting a line that intersects the transfer curve.



Week - 6

Voltage-Divider Q-point

Step 1

Plot the line by plotting two points:

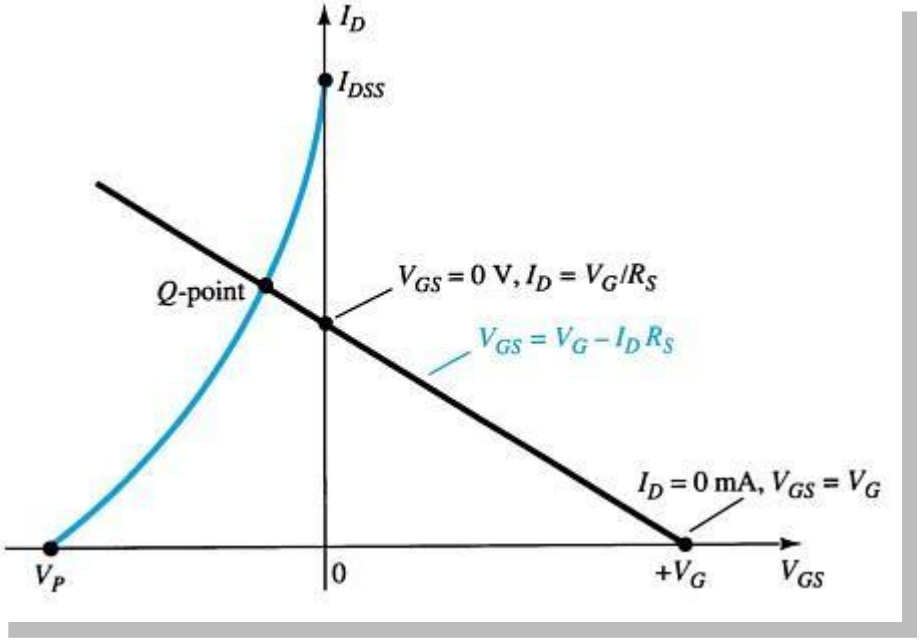
- **$V_{GS} = V_G$, $I_D = 0$ A**
- **$V_{GS} = 0$ V, $I_D = V_G / R_S$**

Step 2

Plot the transfer curve by plotting I_{DSS}, V_P and the calculated values of I_D

Step 3

The Q-point is located where the line intersects the transfer curve



Voltage-Divider Bias Calculations

Using the value of I_D at the Q-point, solve for the other variables in the voltage-divider bias circuit:

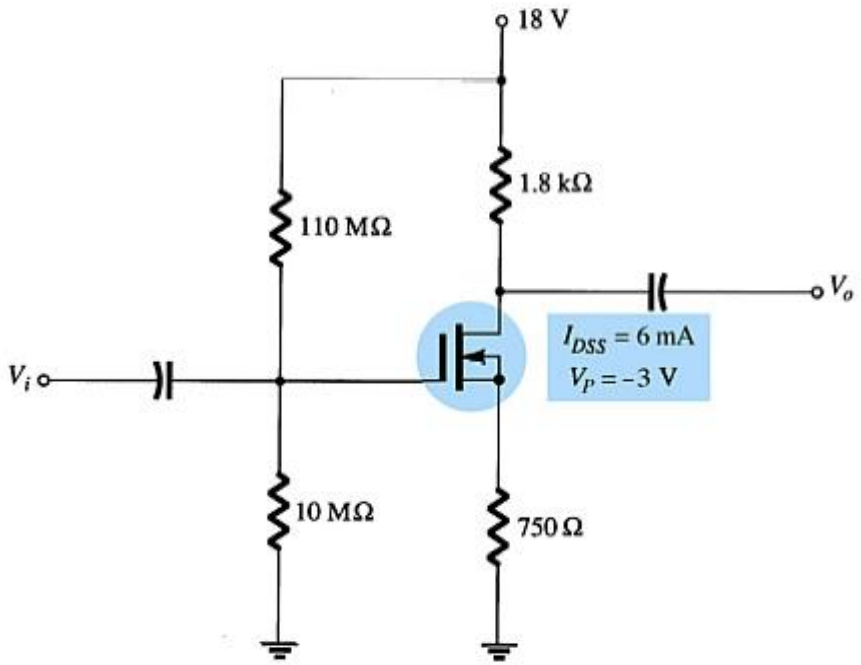
$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = I_D R_S$$

$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

Depletion-type MOSFET bias circuits are similar to those used to bias JFETs. The only difference is that depletion-type MOSFETs can operate with positive values of V_{GS} and with I_D values that exceed I_{DSS}.



Step 1

Plot line for

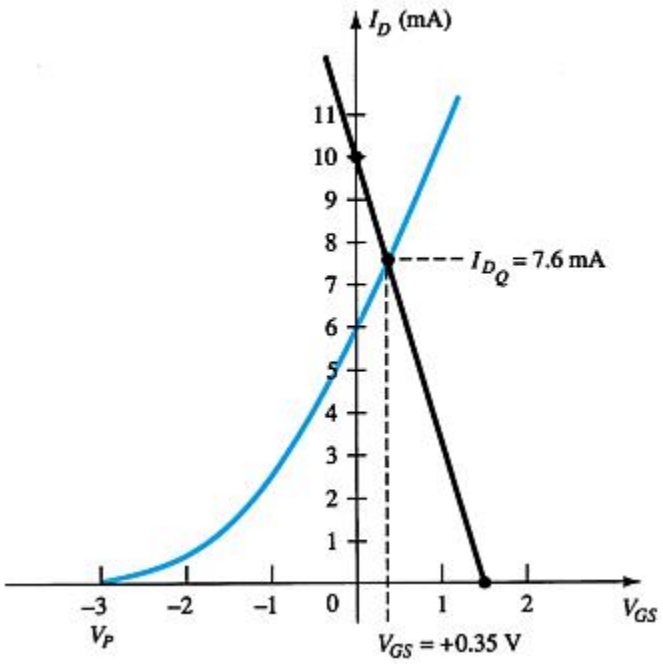
- **$V_{GS} = V_G$, $I_D = 0$ A**
- **$I_D = V_G/R_S$, $V_{GS} = 0$ V**

Step 2

Plot the transfer curve using I_{DSS}, V_P and calculated values of I_D

Step 3

The Q-point is located where the line intersects the transfer curve. Use the I_D at the Q-point to solve for the other variables in the voltage-divider bias circuit.



These are the same steps used to analyze JFET self-bias circuits.

Voltage-Divider Bias

Step 1

Plot the line for

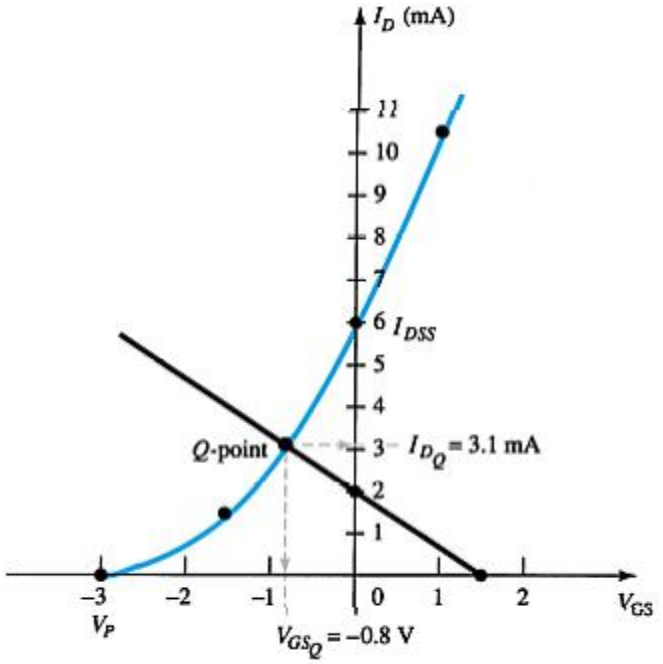
- **$V_{GS} = V_G$, $I_D = 0$ A**
- **$I_D = V_G/R_S$, $V_{GS} = 0$ V**

Step 2

Plot the transfer curve using I_{DSS}, V_P and calculated values of I_D.

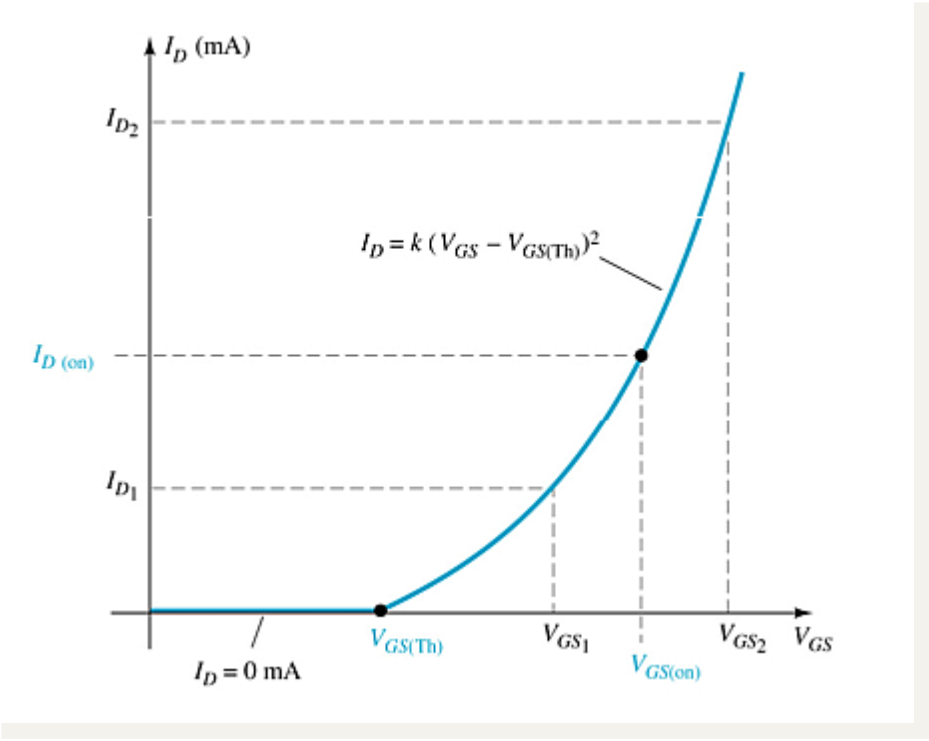
Step 3

The Q-point is located where the line intersects the transfer curve is. Use the I_D at the Q-point to solve for the other variables in the voltage-divider bias circuit.



These are the same steps used to analyze JFET voltage-divider bias circuits.

The transfer characteristic for the e-type MOSFET is very different from that of a simple JFET or the d-type MOSFET.



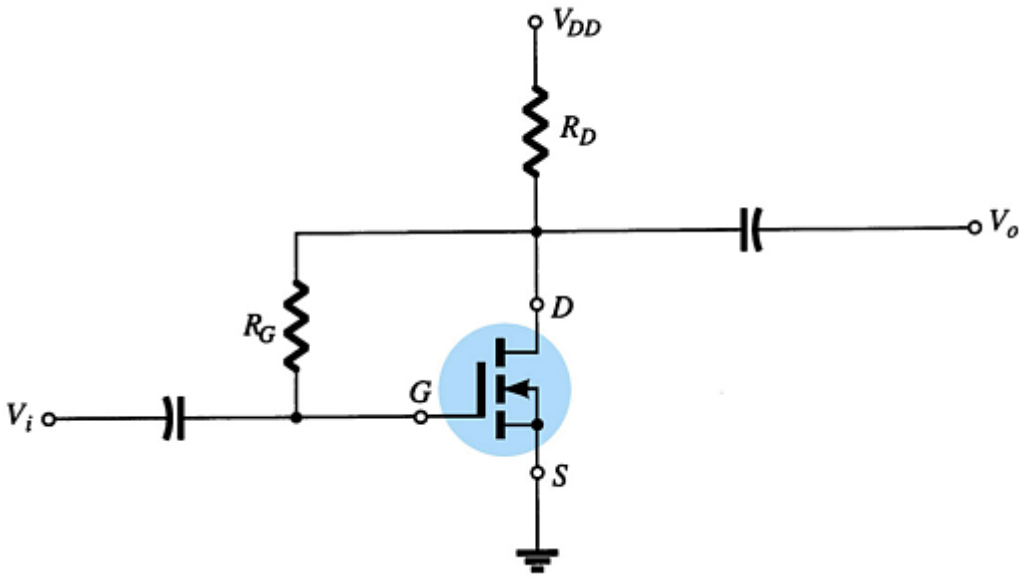
Feedback Bias Circuit

$I_G = 0\ A$

$V_{RG} = 0\ V$

$V_{DS} = V_{GS}$

$V_{GS} = V_{DD} - I_D R_D$



Step 1

Plot the line using

- **$V_{GS} = V_{DD}$, $I_D = 0$ A**
- **$I_D = V_{DD} / R_D$, $V_{GS} = 0$ V**

Step 2

Using values from the specification sheet, plot the transfer curve with

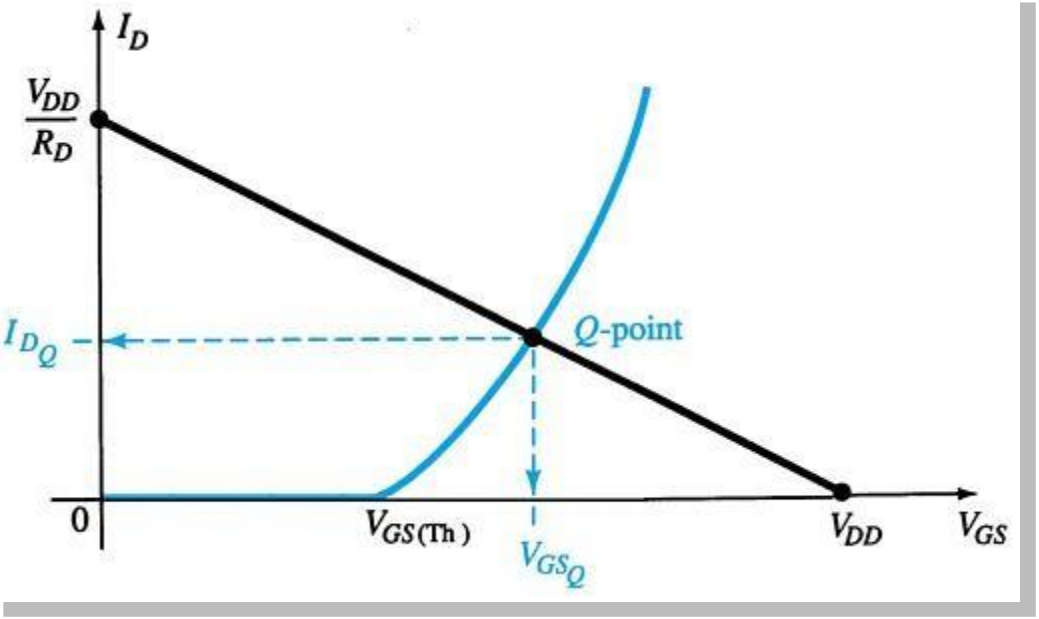
- **V_{GSTh} , $I_D = 0$ A**
- **$V_{GS(on)}$, $I_{D(on)}$**

Step 3

The Q-point is located where the line and the transfer curve intersect

Step 4

Using the value of I_D at the Q-point, solve for the other variables in the bias circuit

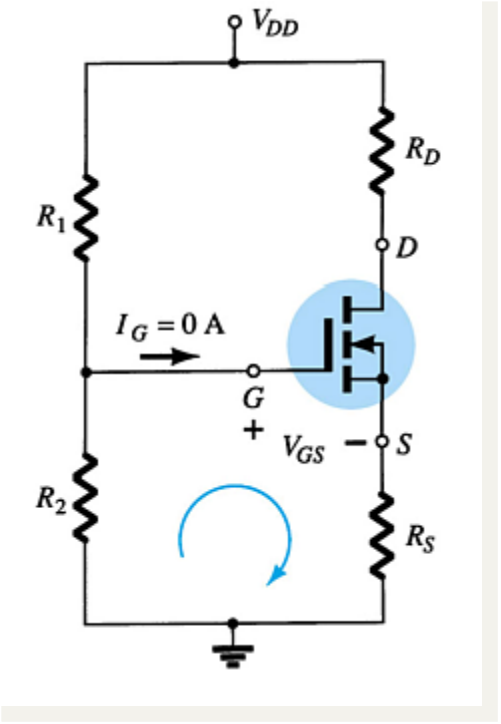


Plot the line and the transfer curve to find the Q-point. Use these equations:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_S + R_D)$$



Step 1

Plot the line using

- **$V_{GS} = V_G = (R_2V_{DD}) / (R_1 + R_2)$, $I_D = 0$ A**
- **$I_D = V_G/R_S$, $V_{GS} = 0$ V**

Step 2

Using values from the specification sheet, plot the transfer curve with

- **V_{GSTh}, $I_D = 0$ A**
- **$V_{GS(on)}$, $I_{D(on)}$**

Step 3

The point where the line and the transfer curve intersect is the Q-point.

Step 4

Using the value of I_D at the Q-point, solve for the other circuit values.

Week - 7

Voltage-controlled resistor
JFET voltmeter
Timer network
Fiber optic circuitry
MOSFET relay driver

- **Approach 1: Graphical solution**
  - **Draw line for V_{GS}**
  - **Draw transfer curve**
  - **Find intersection**

- **Approach 2: Mathematical Solution**
  - **Solve the two equations**
    - **VGS**
    - **Transfer equation**

Introduction

FETs provide:

- **Excellent voltage gain**
- **High input impedance**
- **Low-power consumption**
- **Good frequency range**

FET Small-Signal Model

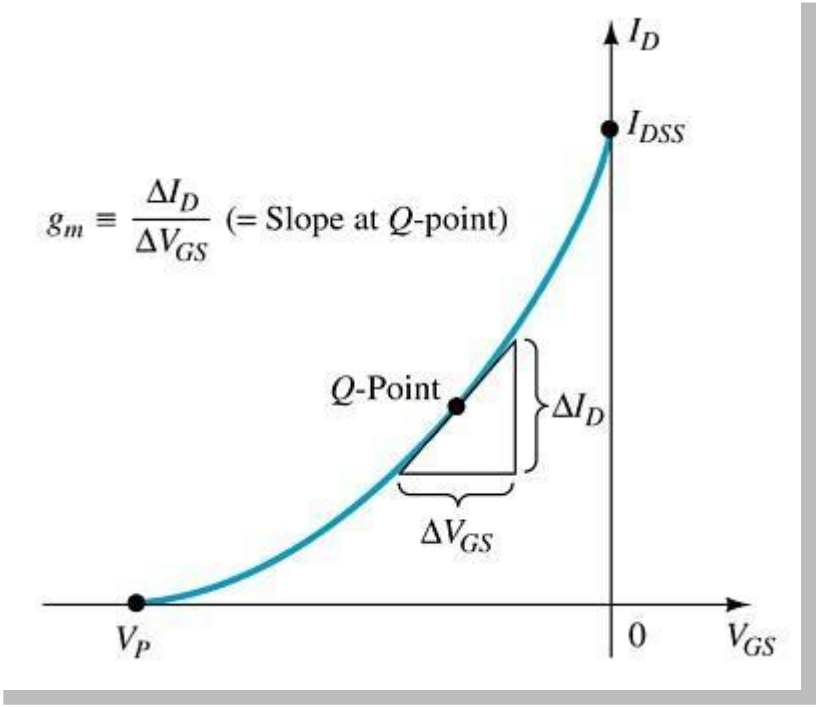
Transconductance

The relationship of a change in I_D to the corresponding change in V_{GS} is called transconductance

Transconductance is denoted g_m and given by:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Graphical Determination of g_m



Mathematical Definitions of g_m

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

Where $V_{GS} = 0V$ $\quad g_{m0} = \frac{2I_{DSS}}{|V_P|}$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

Where $\quad 1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

FET Impedance

Input impedance:

$$Z_i = \infty\ \Omega$$

Output Impedance:

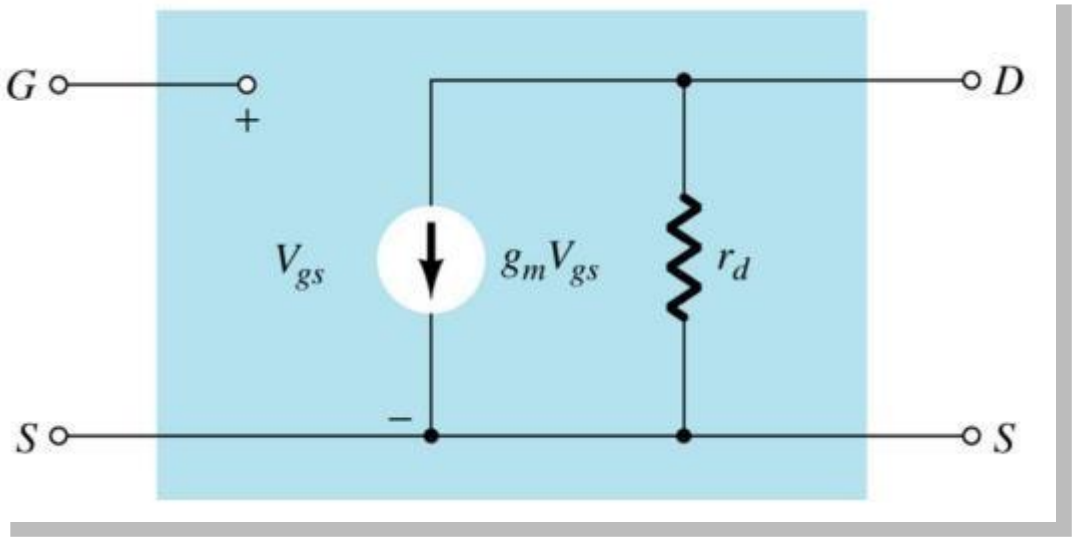
$$Z_o = r_d = \frac{1}{y_{os}}$$

where:

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}\ =\ \text{constant}}$$

y_{os}= admittance parameter listed on FET specification sheets.

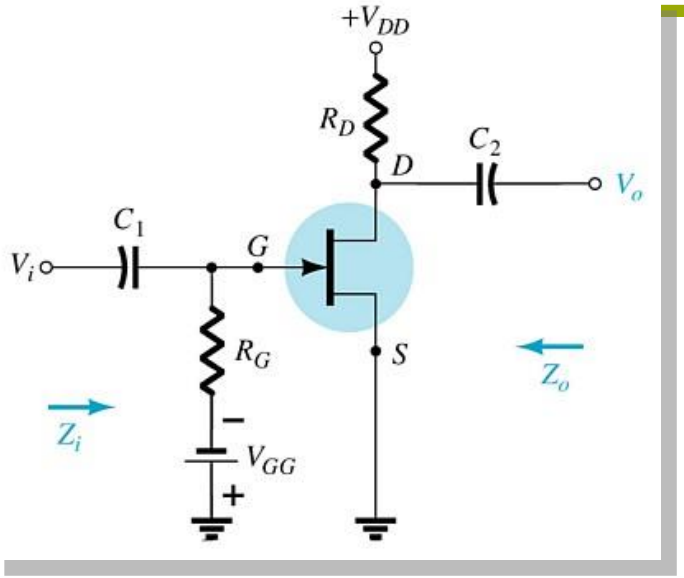
FET AC Equivalent Circuit

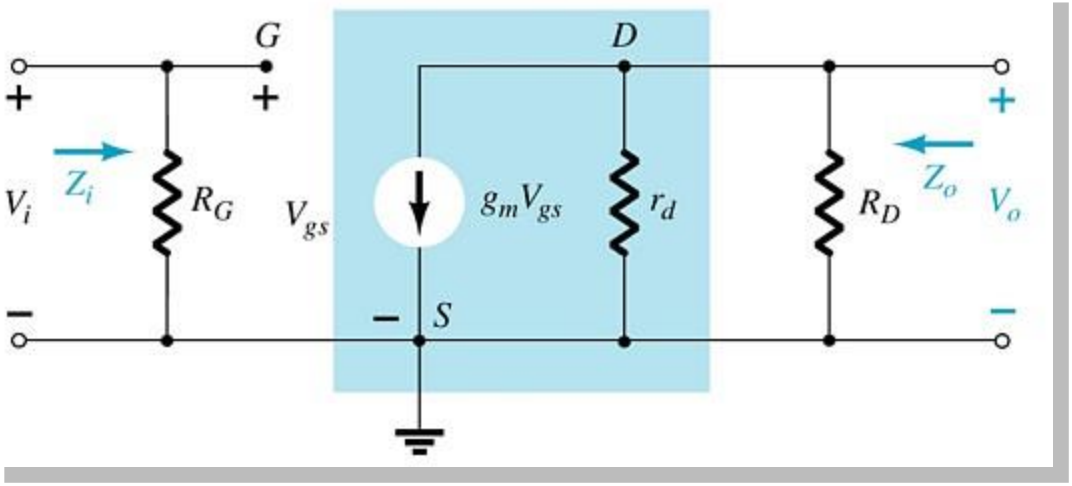


Common-Source (CS) Fixed-Bias Circuit

The input is on the gate and the output is on the drain

There is a 180° phase shift between input and output





Week - 8

Calculations

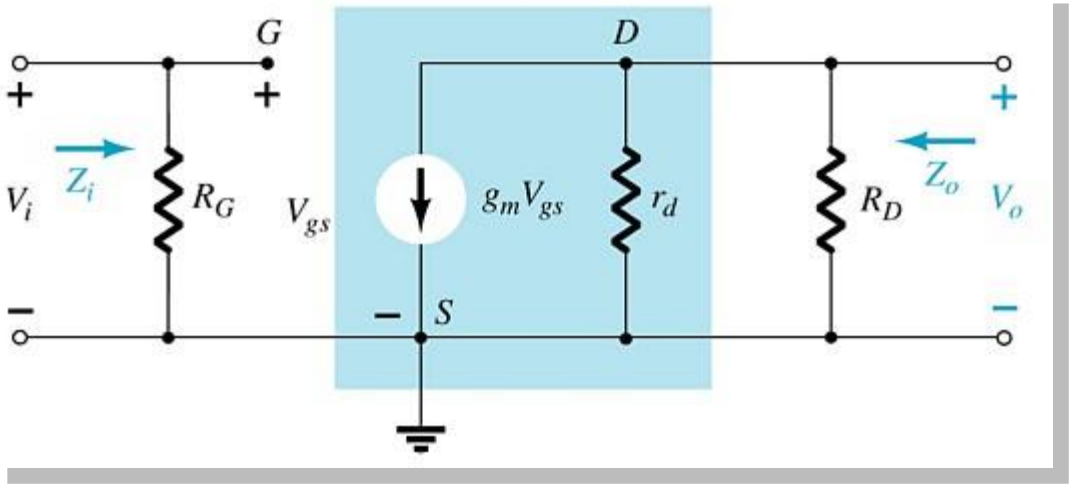
Input impedance:

$$Z_i = R_G$$

Output impedance:

$$Z_o = R_D \parallel r_d$$

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$



Voltage gain:

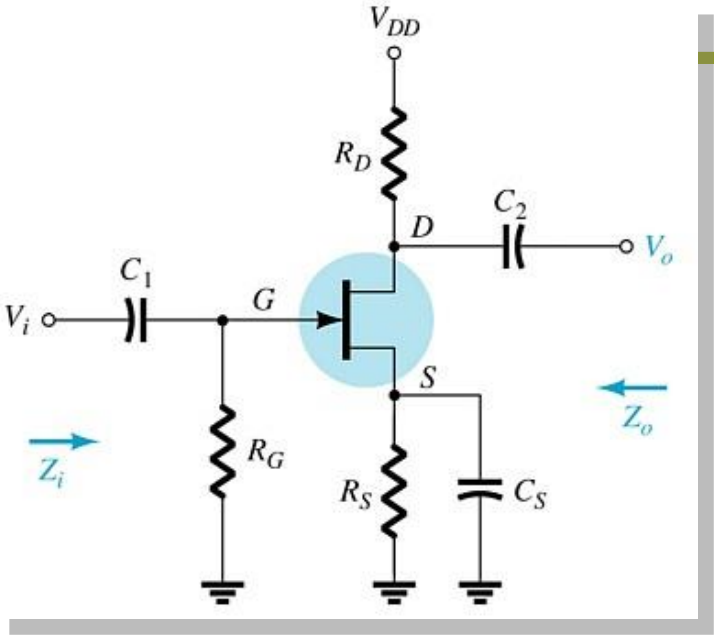
$$A_v = \frac{V_o}{V_i} = -g_m (r_d \parallel R_D)$$

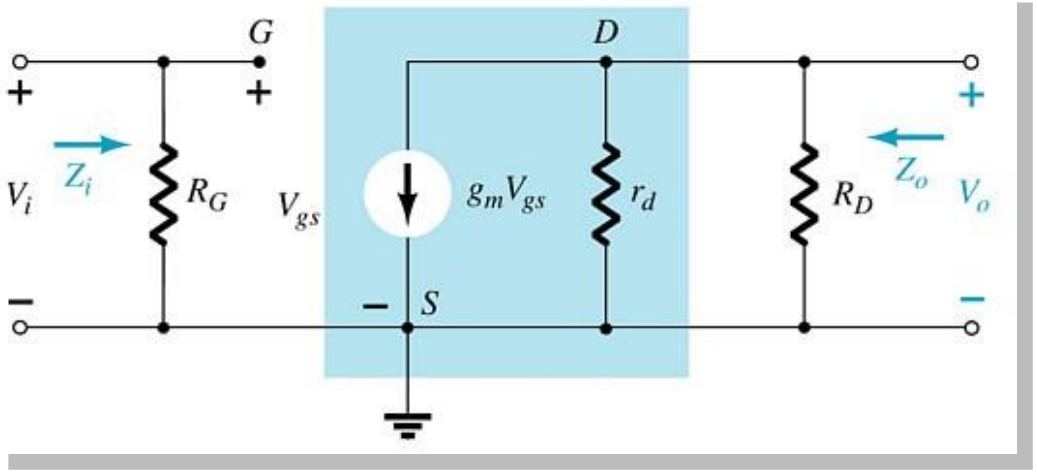
$$A_v = \frac{V_o}{V_i} = -g_m R_D \Big|_{r_d \geq 10R_D}$$

Common-Source (CS) Self-Bias Circuit

This is a common-source amplifier configuration, so the input is on the gate and the output is on the drain

There is a 180° phase shift between input and output





Calculations

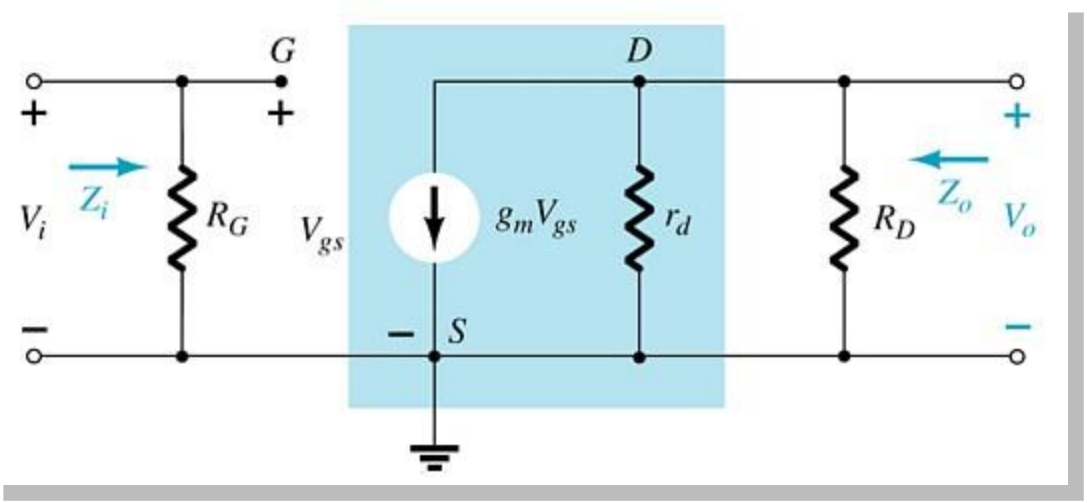
Input impedance:

$$Z_i = R_G$$

Output impedance:

$$Z_o = r_d \parallel R_D$$

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$



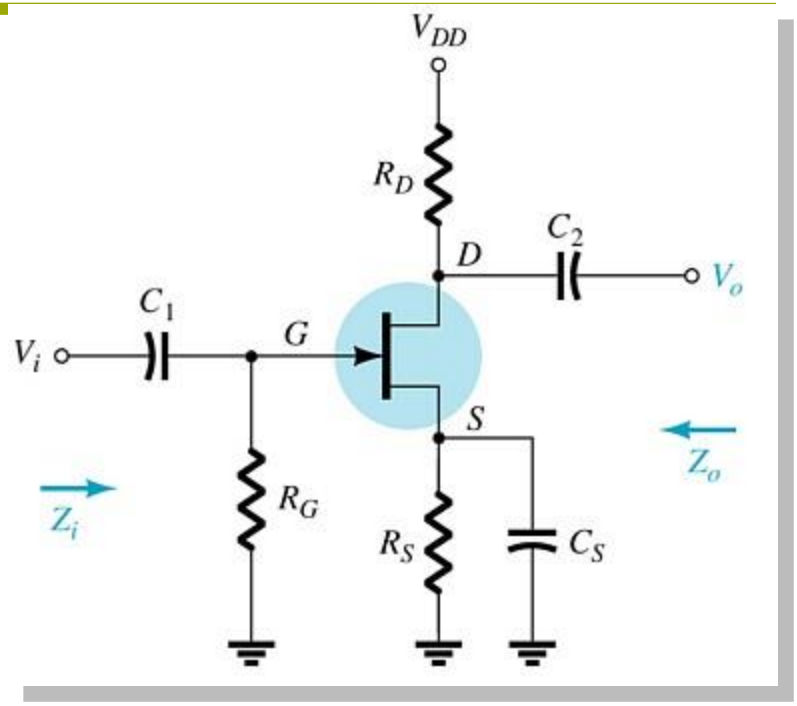
Voltage gain:

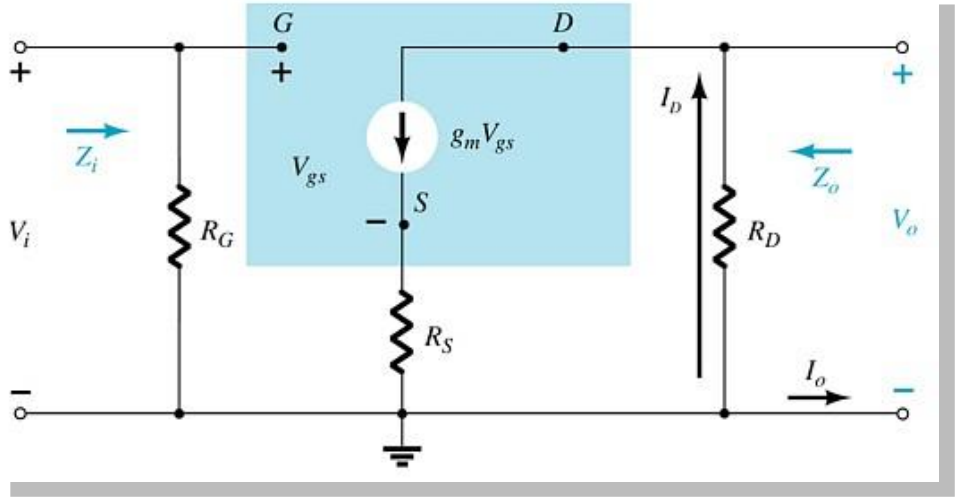
$$A_v = -g_m (r_d \parallel R_D)$$

$$A_v = -g_m R_D \Big|_{r_d \geq 10R_D}$$

Common-Source (CS) Self-Bias Circuit

Removing C_s affects the gain of the circuit.





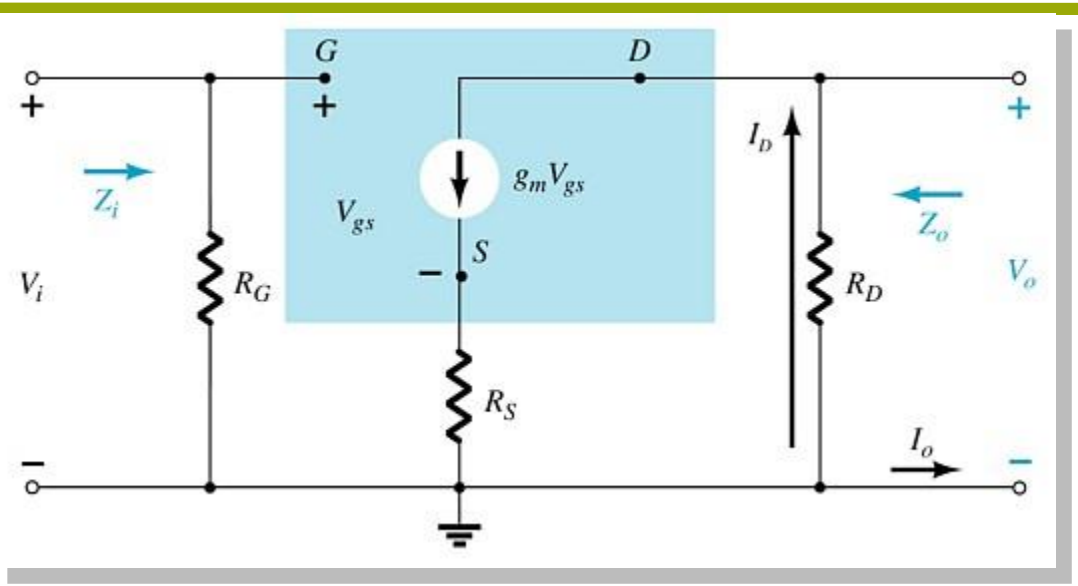
Calculations

Input impedance:

$$Z_i = R_G$$

Output impedance:

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$



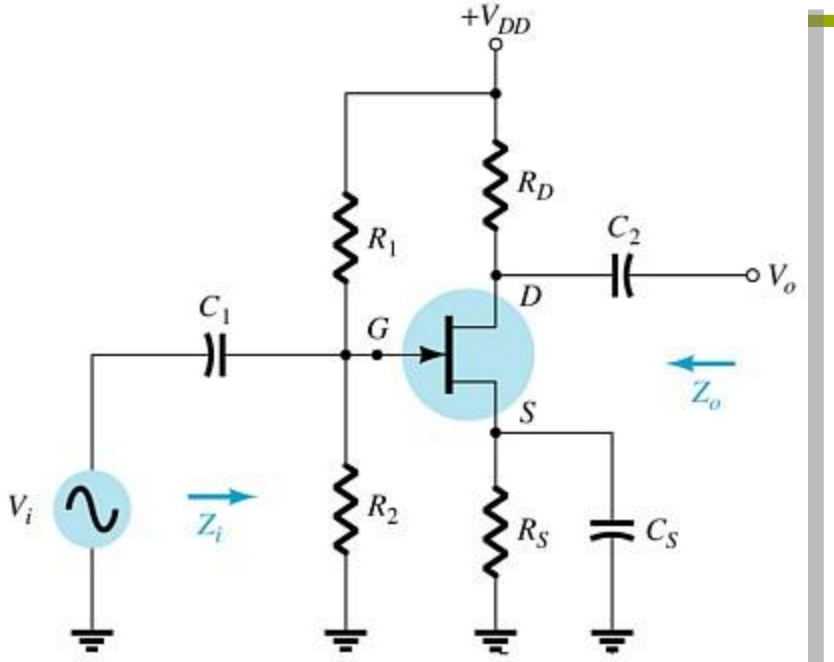
Voltage gain:

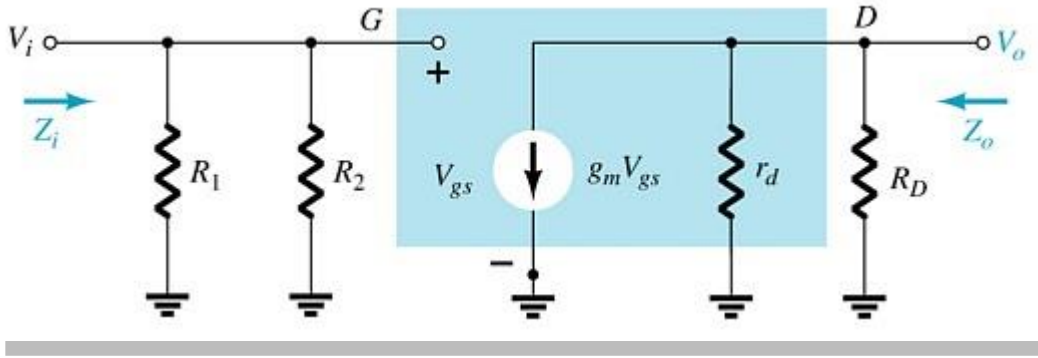
$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$$

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S}\Bigg|_{r_d \geq 10(R_D + R_S)}$$

Common-Source (CS) Voltage-Divider Bias

This is a common-source amplifier configuration, so the input is on the gate and the output is on the drain.





Impedances

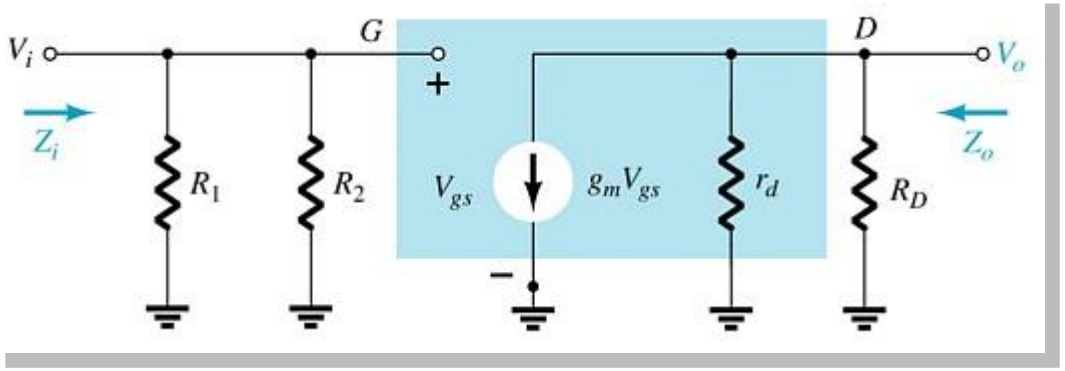
Input impedance:

$$Z_i = R_1 \parallel R_2$$

Output impedance:

$$Z_o = r_d \parallel R_D$$

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$



Voltage gain:

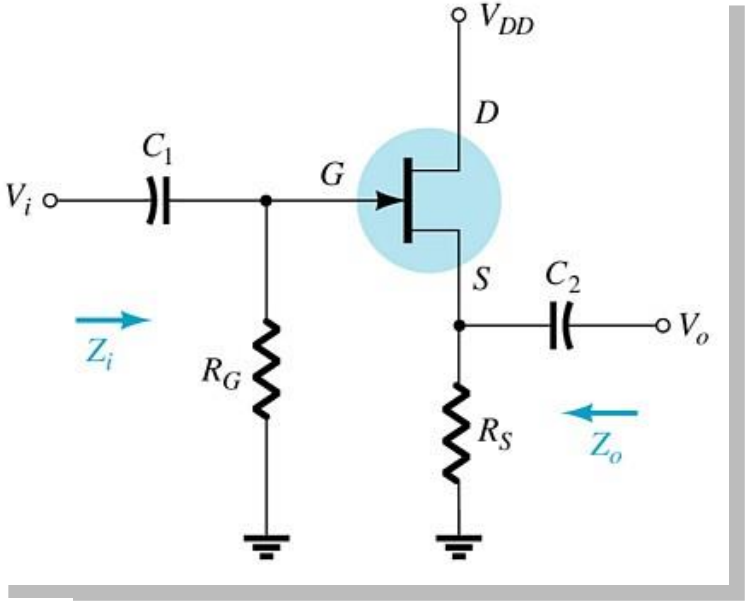
$$A_v = -g_m (r_d \parallel R_D)$$

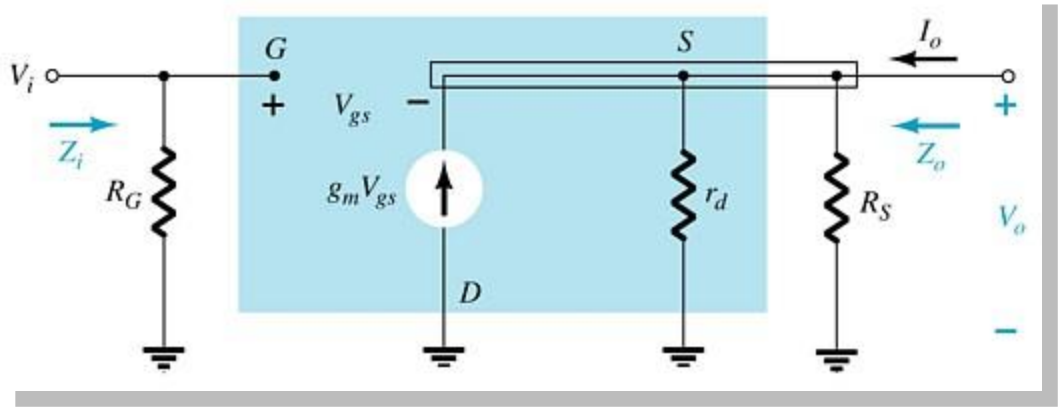
$$A_v = -g_m R_D \Big|_{r_d \geq 10R_D}$$

Source Follower (Common-Drain) Circuit

In a common-drain amplifier configuration, the input is on the gate, but the output is from the source.

There is no phase shift between input and output.

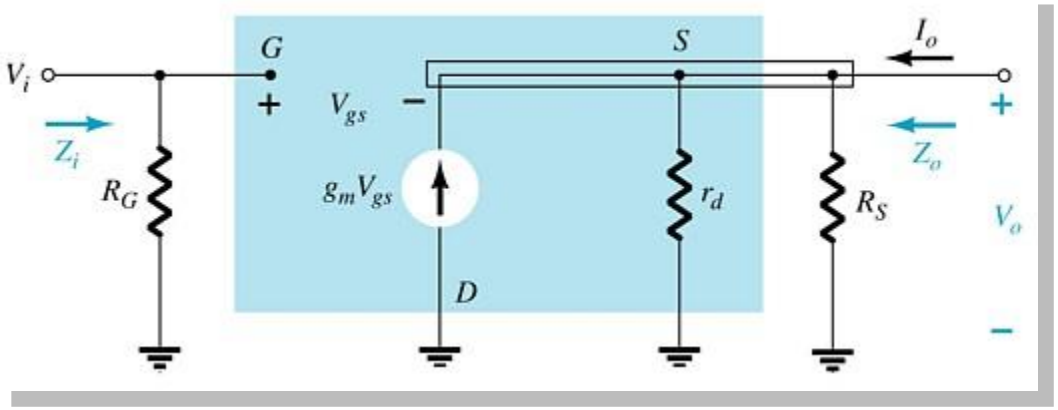




Impedances

Input impedance:

$$Z_i = R_G$$



Output impedance:

$$Z_o = r_d \parallel R_S \parallel \frac{1}{g_m}$$

$$Z_o \cong R_S \parallel \frac{1}{g_m} \Big| \; r_d \geq 10 R_S$$

Voltage gain:

$$A_v = \frac{V_o}{V_i} = \frac{g_m (r_d \parallel R_S)}{1 + g_m (r_d \parallel R_S)}$$

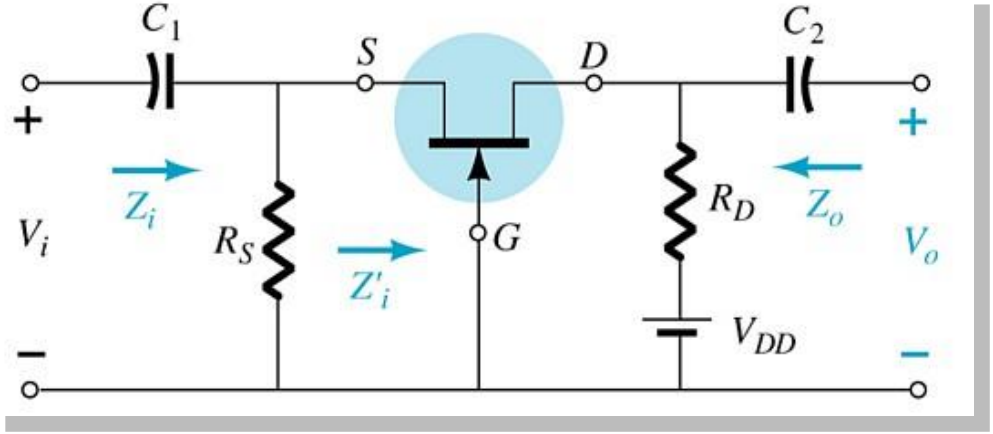
$$A_v = \frac{V_o}{V_i} = \frac{g_m R_S}{1 + g_m R_S} \Big| r_d \geq 10$$

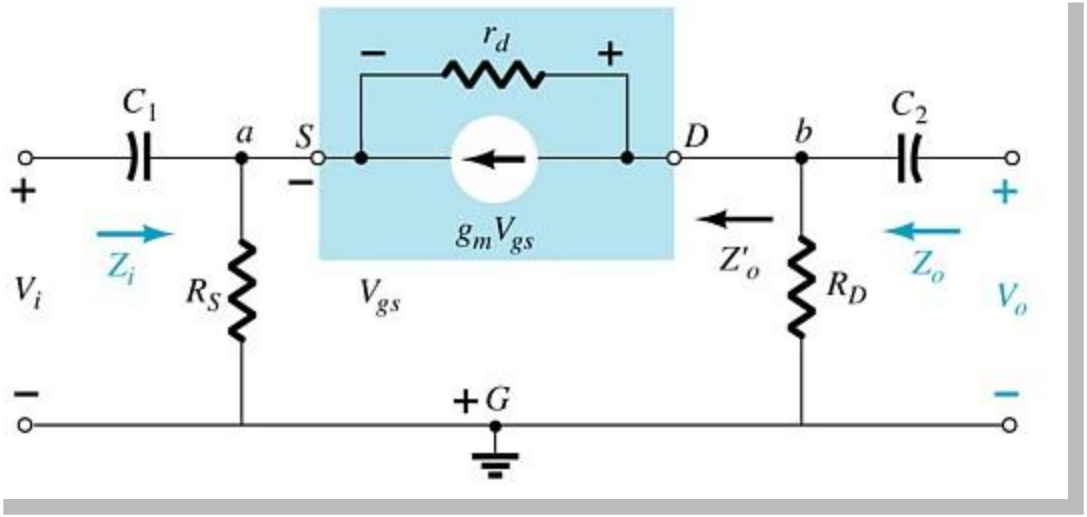
Week - 9

Common-Gate (CG) Circuit

The input is on the source and the output is on the drain.

There is no phase shift between input and output.



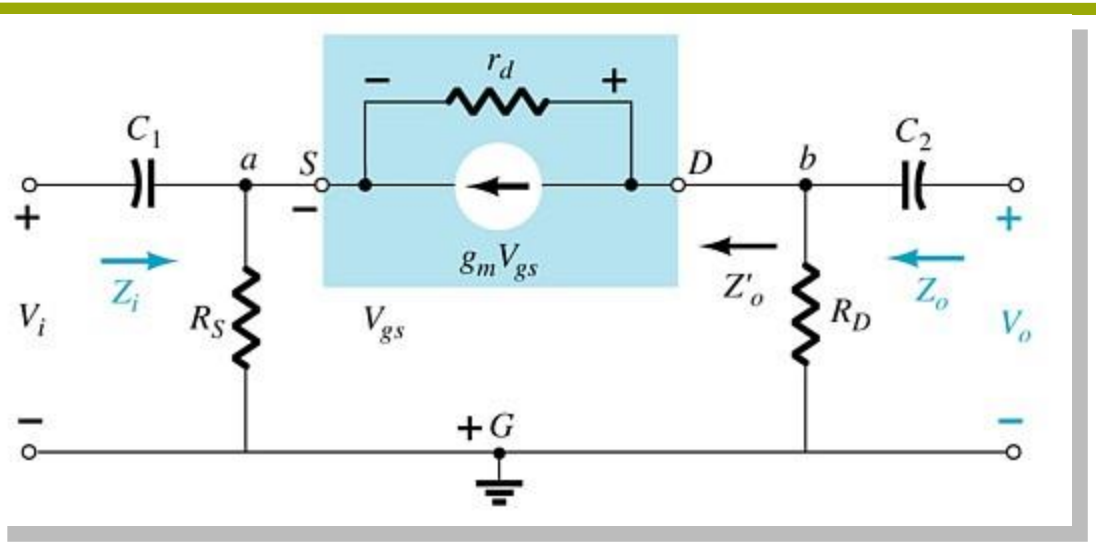


Calculations

Input impedance:

$$Z_i = R_S \parallel \left[\frac{r_d + R_D}{1 + g_m r_d}\right]$$

$$Z_i \cong R_S \parallel \frac{1}{g_m}\Big|_{r_d \geq 10R_D}$$



Output impedance:

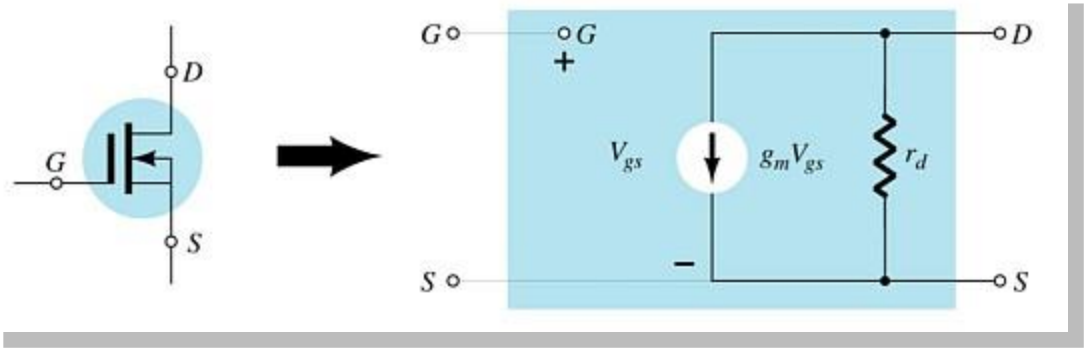
$$Z_o = R_D \parallel r_d$$

$$Z_o \cong R_D\Big|_{r_d \geq 10}$$

Voltage gain:

$$A_v = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]} \qquad A_v = g_m R_D\Big|_{r_d \geq 10R_D}$$

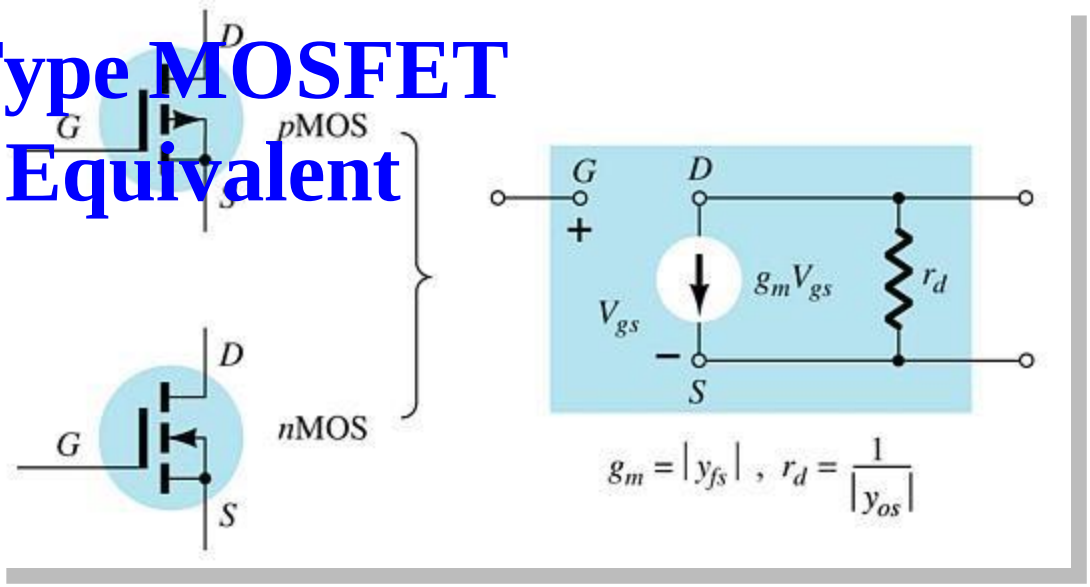
D-Type MOSFET AC Equivalent



E-Type MOSFET AC Equivalent

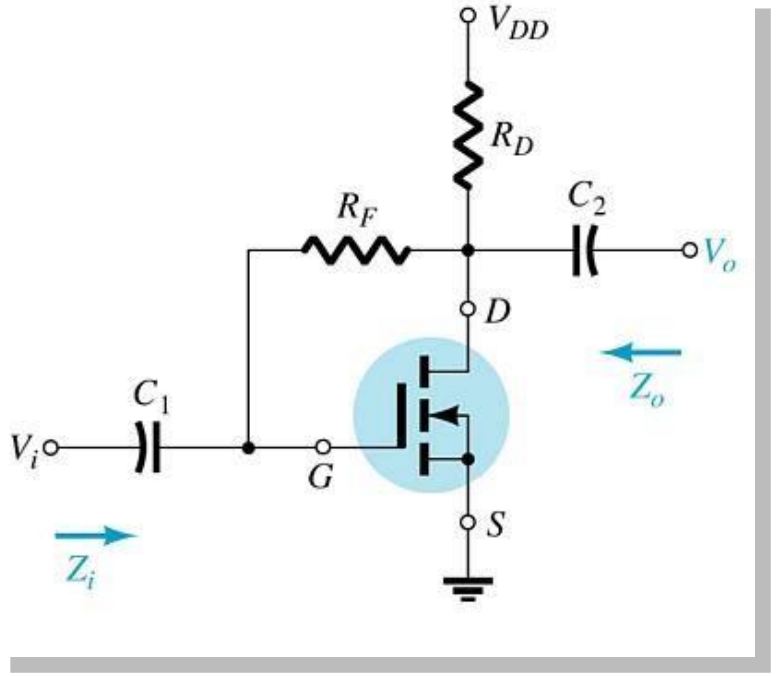
g_m and r_d can be found in the specification sheet for the FET.

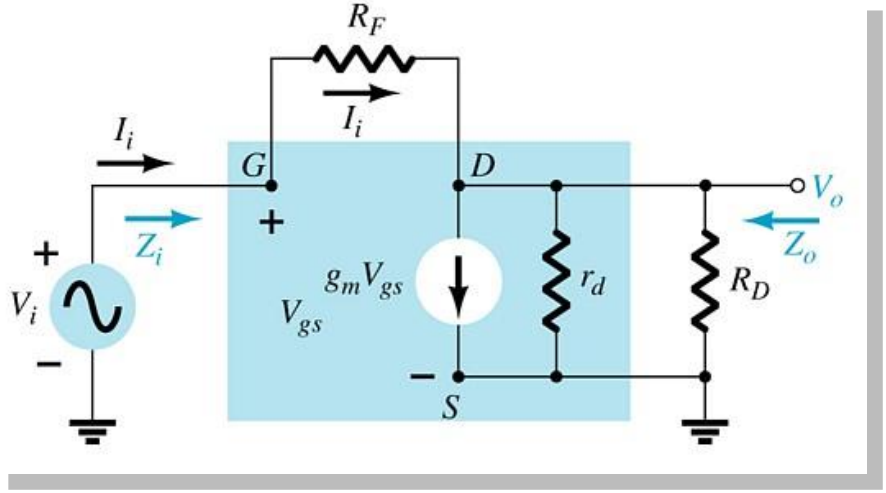
E-Type MOSFET AC Equivalent



Common-Source Drain-Feedback

There is a 180° phase shift between input and output.





Calculations

Input impedance:

$$Z_i = \frac{R_F + r_d \,||\, R_D}{1 + g_m (r_d \,||\, R_D)}$$

$$Z_i \cong \frac{R_F}{1 + g_m R_D} \Big|_{R_F >> r_d || R_D, r_d \geq 10 R_D}$$

Output impedance:

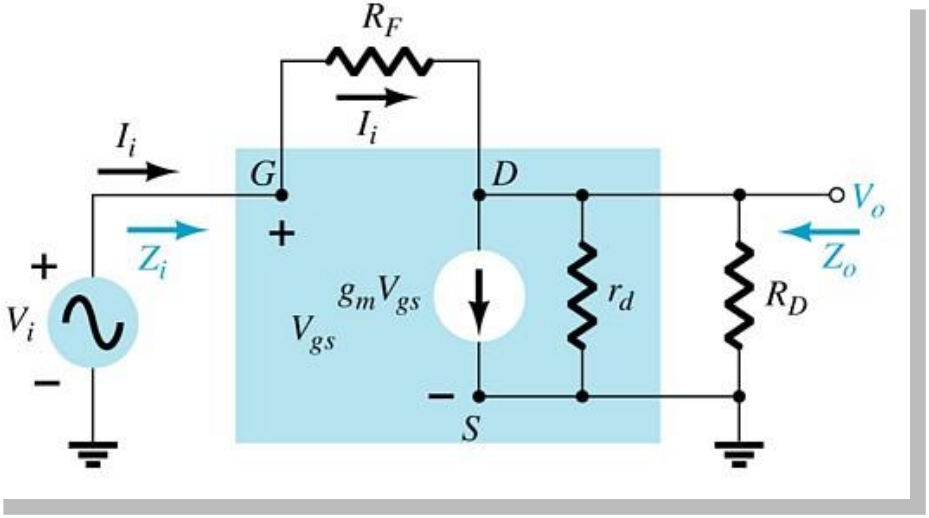
$$Z_o = R_F \,||\, r_d \,||\, R_D$$

$$Z_o \cong R_D \Big|_{R_F >> r_d || R_D, r_d \geq 10 R_D}$$

Voltage gain:

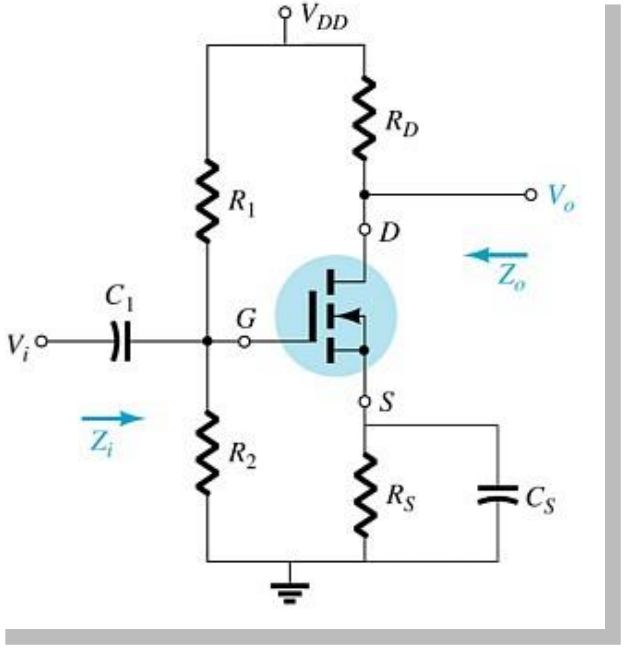
$$A_v = -g_m (R_F \,||\, r_d \,||\, R_D)$$

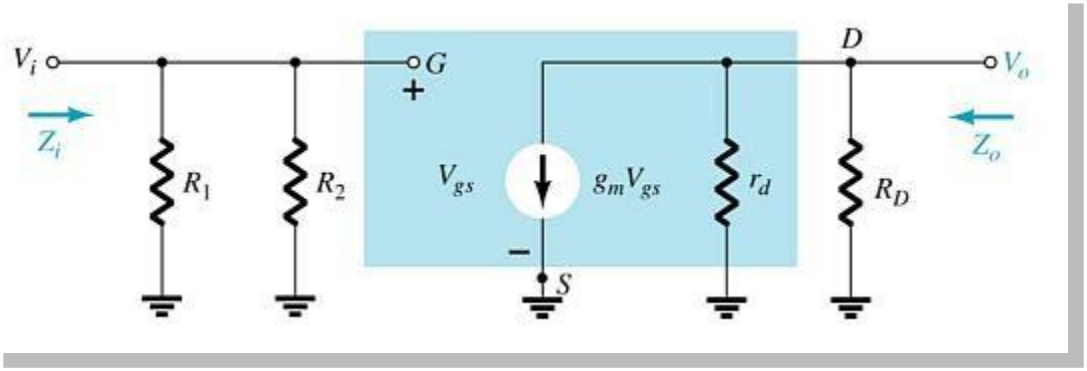
$$A_v \cong -g_m R_D \Big|_{R_F >> r_d || R_D, r_d \geq 10 R_D}$$



Week - 10

Common-Source Voltage-Divider Bias





Calculations

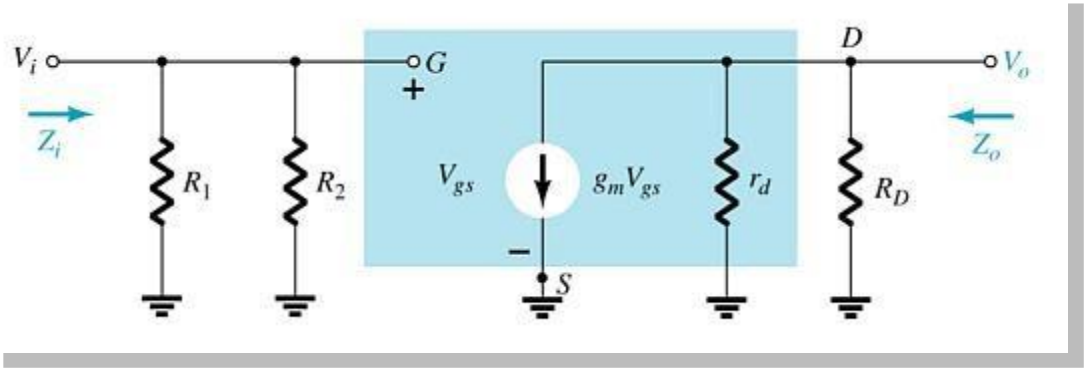
Input impedance:

$$Z_i = R_1 \| R_2$$

Output impedance:

$$Z_o = r_d \| R_D$$

$$Z_o \cong R_D \Big|_{r_d \geq 10}$$



Voltage gain:

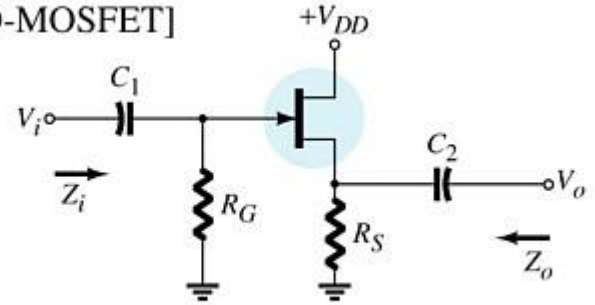
$$A_v = -g_m (r_d \| R_D)$$

$$A_v \cong -g_m R_D \Big|_{r_d \geq 10 R_D}$$

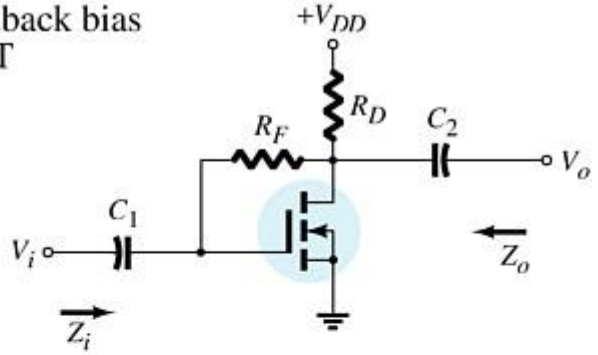
Summary Table

Summary Table

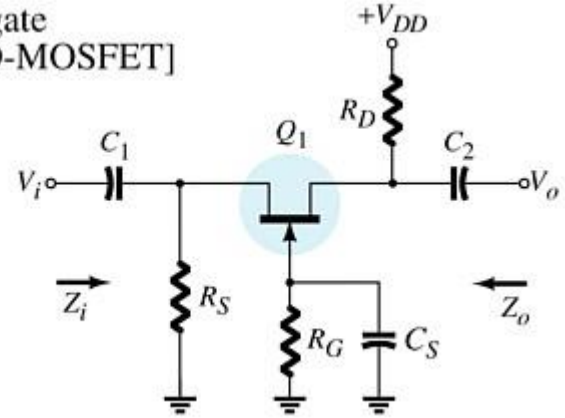
Source-follower
[JFET or D-MOSFET]



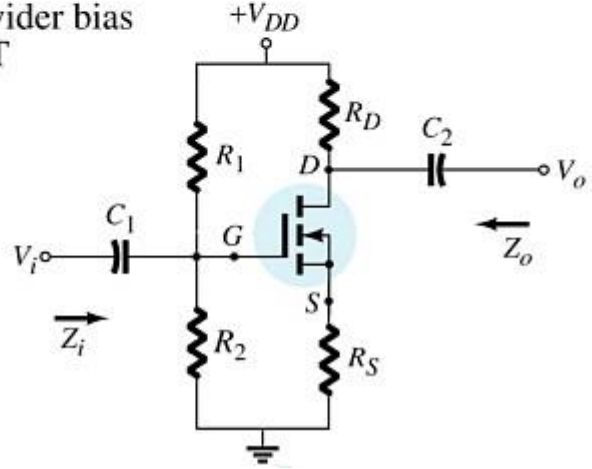
Drain-Feedback bias
E-MOSFET



Common-gate
[JFET or D-MOSFET]



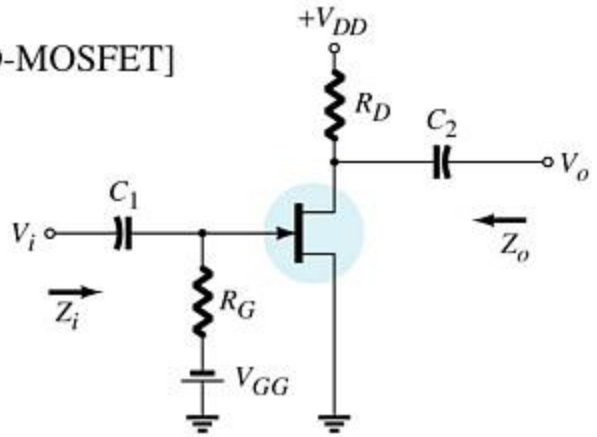
Voltage-divider bias
E-MOSFET



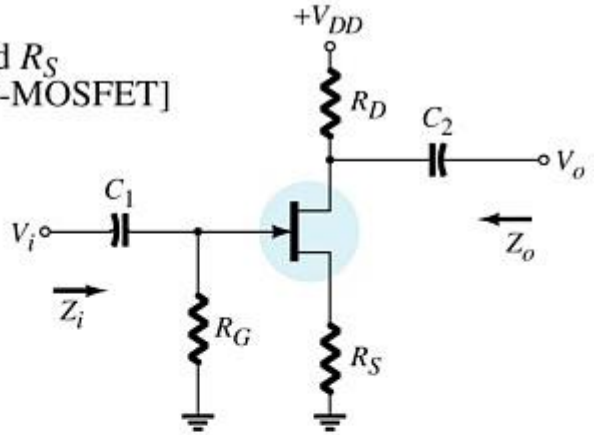
more…

Summary Table

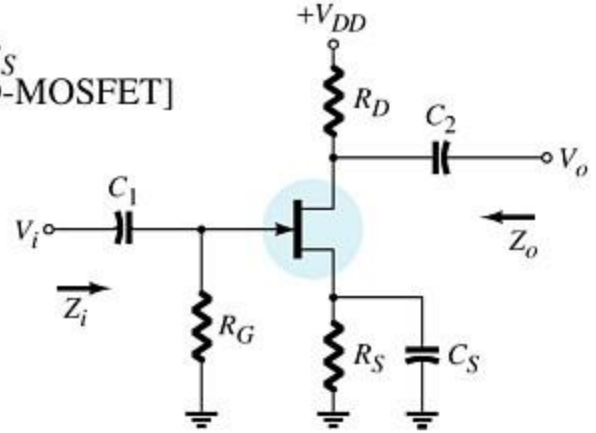
Fixed-bias
[JFET or D-MOSFET]



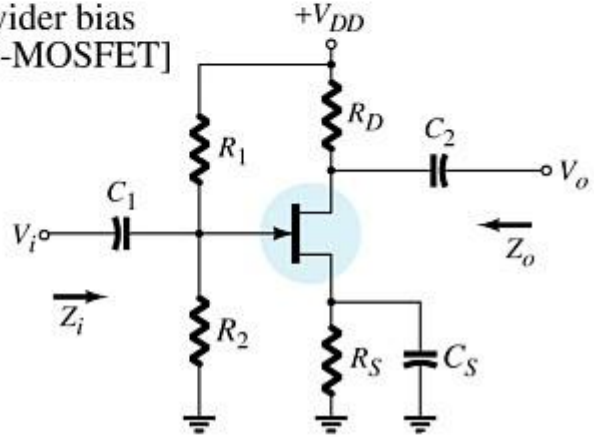
Self-bias
Unbypassed R_S
[JFET or D-MOSFET]



Self-bias
bypassed R_S
[JFET or D-MOSFET]



Voltage-divider bias
[JFET or D-MOSFET]



Troubleshooting

Check the DC bias voltages:

Check the DC bias voltages:

If not correct check power supply, resistors, FET.
Also check to ensure
that the coupling capacitor between amplifier stages is OK.

Check the AC voltages:

.

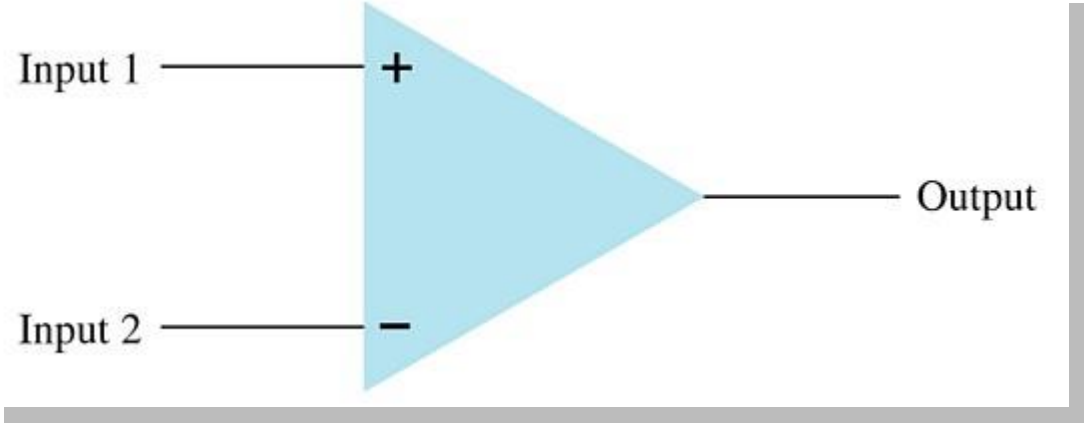
Check the AC voltages:

If not correct check FET, capacitors and the loading effect of the next
stage

Week - 11

EE 2209
Electronics-II
Operational Amplifier

Basic Op-Amp



Operational amplifier or op-amp, is a very high gain differential amplifier with a high input impedance (typically a few meg-Ohms) and low output impedance (less than 100 Ω).

Note the op-amp has two inputs and one output.

A differential amplifier is a type of electronic amplifier that amplifies the difference between two input voltages but suppresses any voltage common to the two inputs.

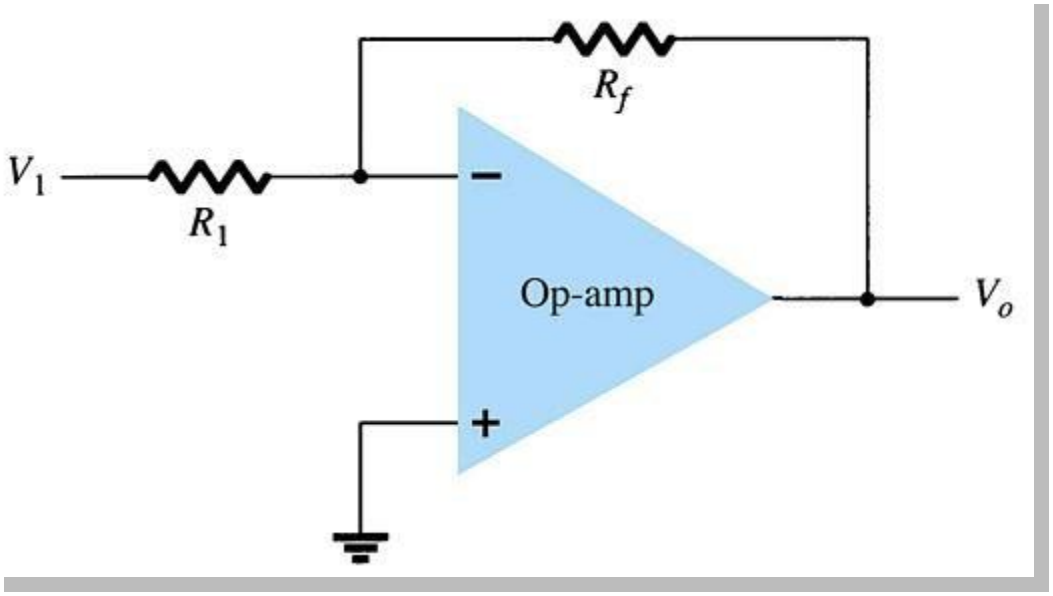
Op-Amp Gain

Op-Amps have a very high gain. They can be connected open-loop or closed-loop.

- **Open-loop refers to a configuration where there is no feedback from output back to the input. In the open-loop configuration the gain can exceed 10,000.**

- **Closed-loop configuration reduces the gain. In order to control the gain of an op-amp it must have feedback. This feedback is a negative feedback. A negative feedback reduces the gain and improves many characteristics of the op-amp.**

Inverting Op-Amp



- **The signal input is applied to the inverting (–) input**
- **The non-inverting input (+) is grounded**
- **The resistor R_f is the feedback resistor. It is connected from the output to the negative (inverting) input. This is *negative feedback*.**

Inverting Op-Amp Gain

Gain can be determined from external resistors: R_f and R_1

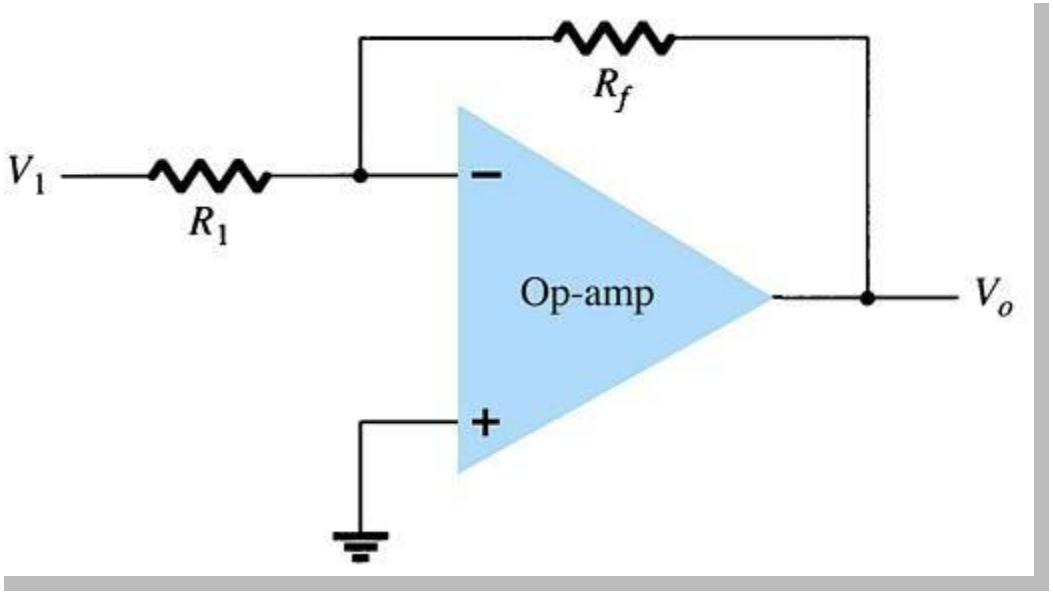
$$A_v = \frac{V_o}{V_i} = \frac{R_f}{R_1}$$

Unity gain—voltage gain is 1

$$R_f = R_1$$

$$A_v = \frac{-R_f}{R_1} = -1$$

The negative sign denotes a 180° phase shift between input and output.

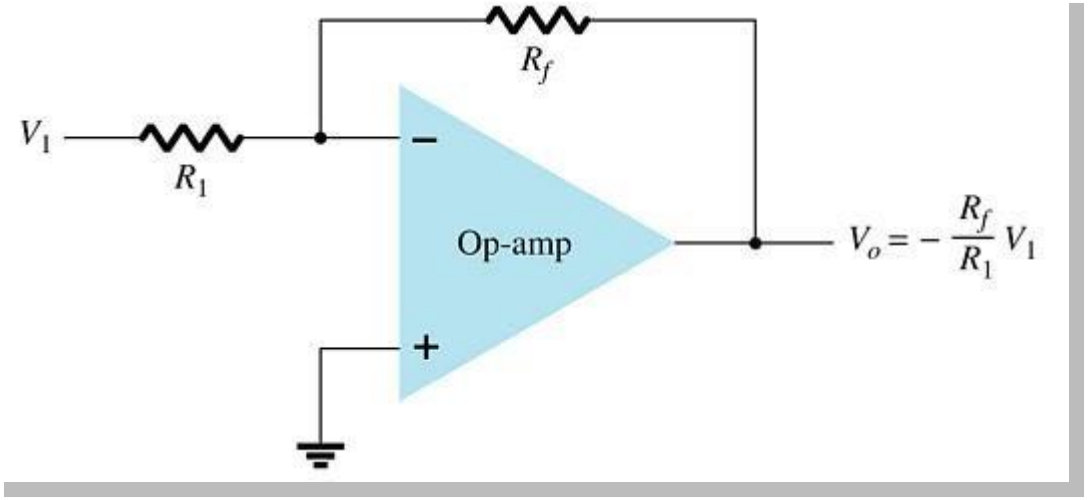


Constant Gain—R_f is a multiple of R_1

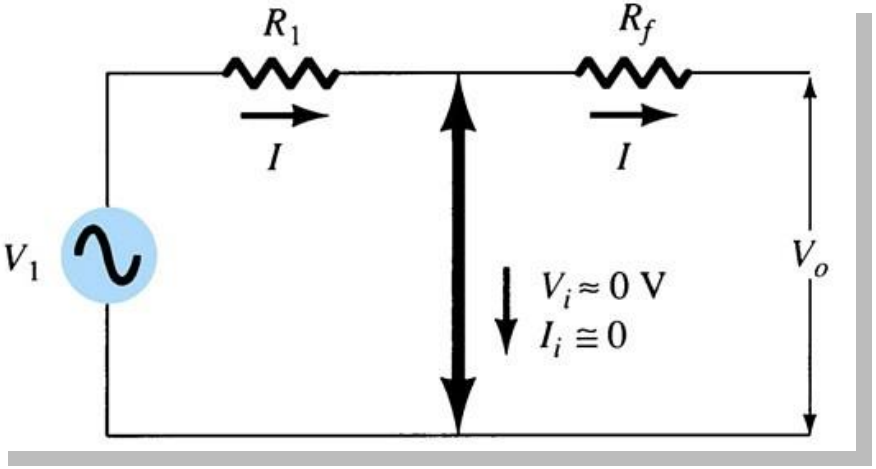
Virtual Ground

An understanding of the concept of virtual ground provides a better understanding of how an op-amp operates.

The *non-inverting* input pin is at ground. *The inverting* input pin is also at 0 V for an AC signal.



The op-amp has such high input impedance that even with a high gain there is no current from inverting input pin, therefore there is no voltage from inverting pin to ground—all of the current is through R_f.



Practical Op-Amp Circuits

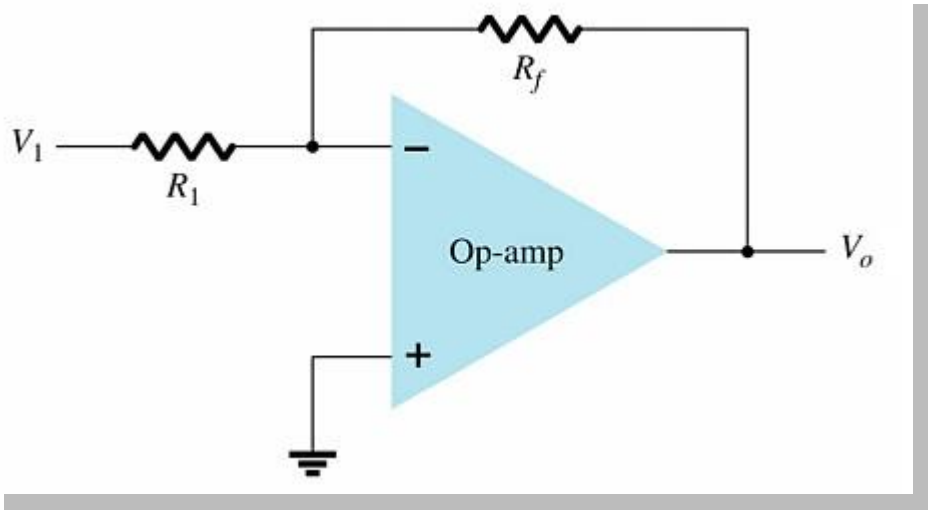
Inverting amplifier
Noninverting amplifier
Unity follower
Summing amplifier
Integrator
Differentiator

Week - 12

Inverting/Noninverting Op-Amps

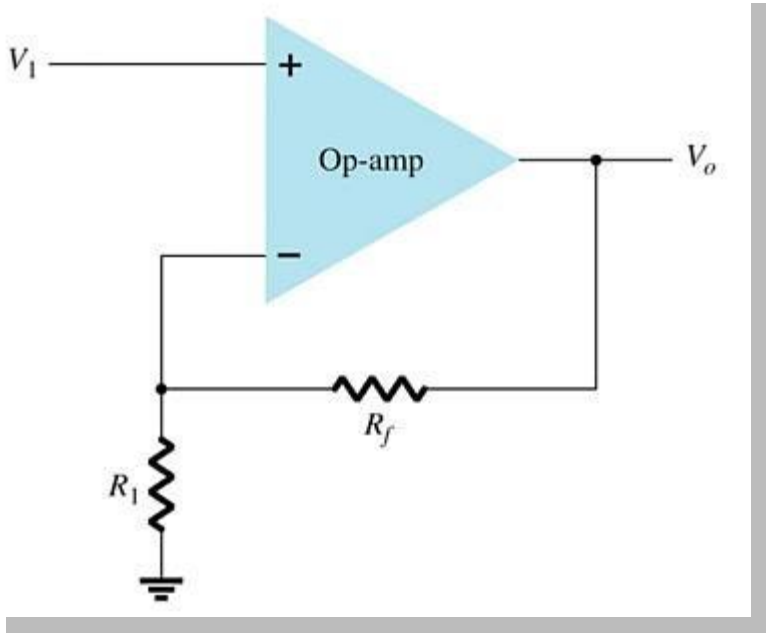
Inverting Amplifier

$$V_o = \frac{-R_f}{R_1} V_1$$



Noninverting Amplifier

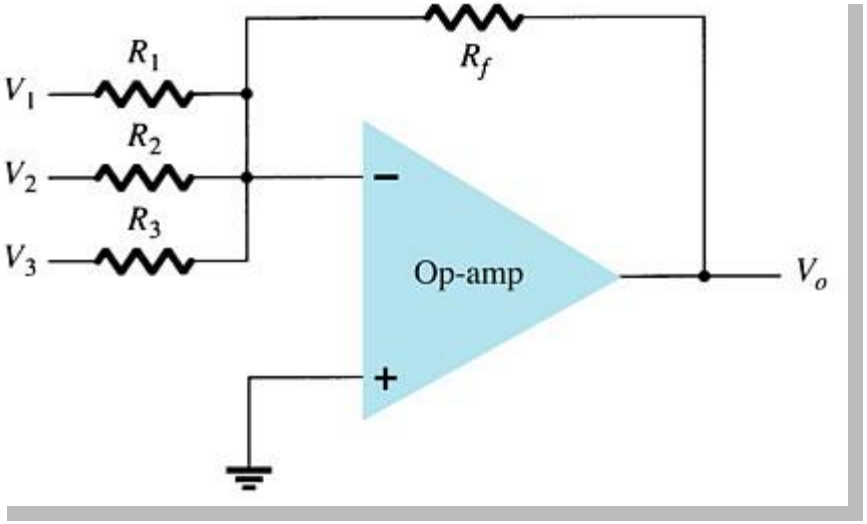
$$V_o = (1 + \frac{R_f}{R_1})V_1$$



Summing Amplifier

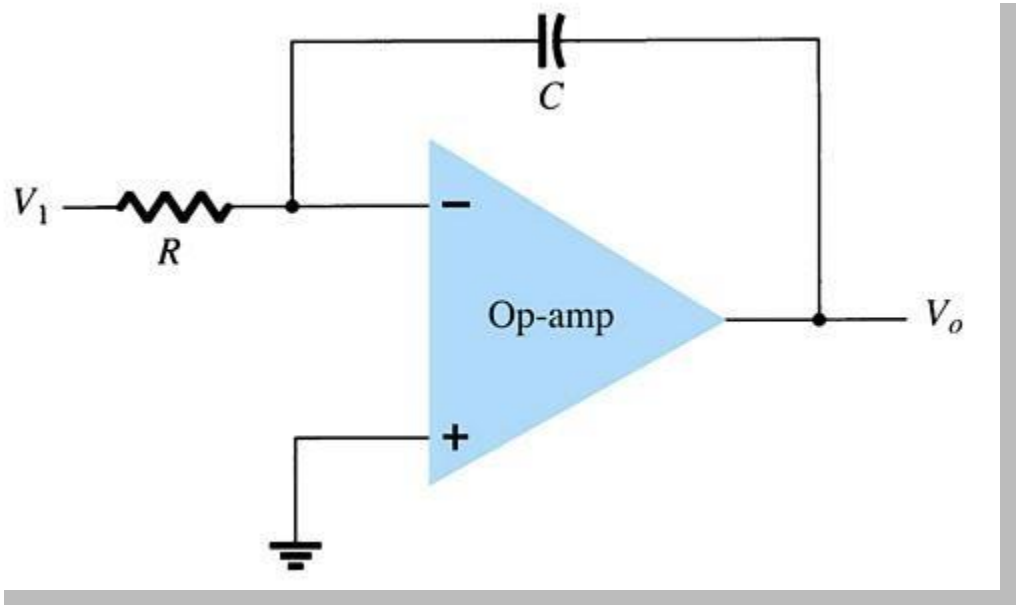
Because the op-amp has a high input impedance, the multiple inputs are treated as separate inputs.

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$



Integrator

The output is the integral of the input. Integration is the operation of summing the area under a waveform or curve over a period of time. This circuit is useful in low-pass filter circuits and sensor conditioning circuits.

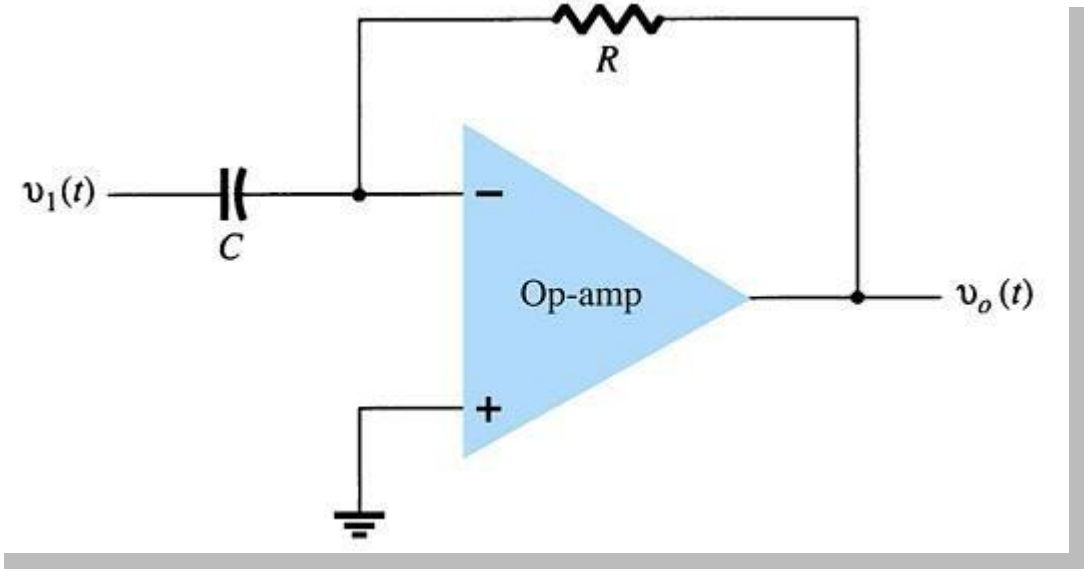


$$v_o(t) = -\frac{1}{RC}\int v_1(t)dt$$

Differentiator

The differentiator takes the derivative of the input. This circuit is useful in high-pass filter circuits.

$$v_o(t) = -RC\frac{dv_1(t)}{dt}$$



Op-Amp Specifications—DC Offset Parameters

Even when the input voltage is zero, there can be an output offset. The following can cause this offset:

- **Input offset voltage**
- **Input offset current**
- **Input offset voltage *and* input offset current**
- **Input bias current**

Output Offset Voltage Due to Input Offset Current (I_{IO})

If there is a difference between the dc bias currents for the same applied input, then this also causes an output offset voltage:

- **The input offset Current (I_{IO}) is specified in the specifications for the op-amp.**
- **The effect on the output can be calculated using:**

$$V_{o(\text{offset due to } I_{IO})} = I_{IO} R_f$$

Week - 13

Total Offset Due to V_{IO} and I_{IO}

Total Offset Due to V_{IO} and I_{IO}

Op-amps may have an output offset voltage due to both factors V_{IO} and I_{IO}. The total output offset voltage will be the sum of the effects of both:

$$V_o(\text{offset}) = V_o(\text{offset due to } V_{IO}) + V_o(\text{offset due to } I_{IO})$$

Input Bias Current (I_{IB})

A parameter that is related to input offset current (I_{IO}) is called input bias current (I_{IB})

The separate input bias currents are:

$$I_{IB}^{-} = I_{IB} - \frac{I_{IO}}{2} \qquad I_{IB}^{+} = I_{IB} + \frac{I_{IO}}{2}$$

The total input bias current is the average:

$$I_{IB} = \frac{I_{IB}^{-} + I_{IB}^{+}}{2}$$

Frequency Parameters

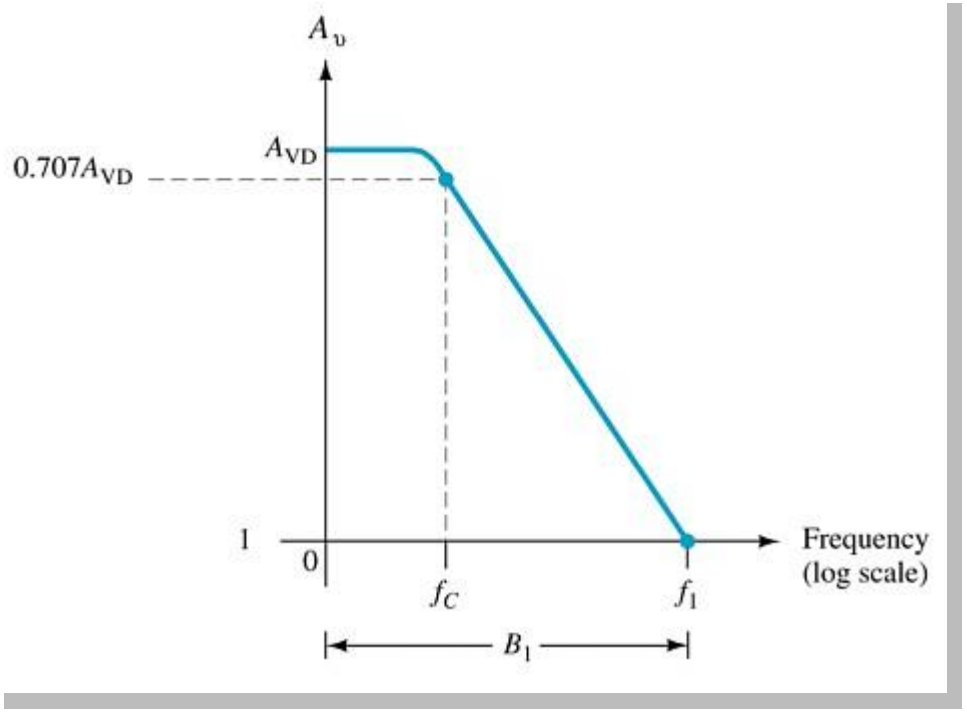
An op-amp is a wide-bandwidth amplifier. The following affect the bandwidth of the op-amp:

- **Gain**
- **Slew rate**

Gain and Bandwidth

The op-amp's high frequency response is limited by internal circuitry. The plot shown is for an open loop gain (A_{OL} or A_{VD}). This means that the op-amp is operating at the highest possible gain with no feedback resistor.

In the open loop, the op-amp has a narrow bandwidth. The bandwidth widens in closed-loop operation, but then the gain is lower.



Slew Rate (SR)

Slew rate (SR) is the maximum rate at which an op-amp can change output without distortion.

$$SR = \frac{\Delta V_o}{\Delta t} \quad \text{(in V/}\mu\text{s)}$$

The SR rating is given in the specification sheets as V/μs rating.

Week - 14

Maximum Signal Frequency

The slew rate determines the highest frequency of the op-amp without distortion.

$$f \leq \frac{SR}{2\pi V_p}$$

where V_P is the peak voltage

General Op-Amp Specifications

Other ratings for op-amp found on specification sheets are:

- **Absolute Ratings**
- **Electrical Characteristics**
- **Performance**

Absolute Ratings

These are common maximum ratings for the op-amp.

Absolute Maximum Ratings	
Supply voltage	6 22 V
Internal power dissipation	500 mW
Differential input voltage	6 30 V
Input voltage	6 15 V

Electrical Characteristics

TABLE 13.2 mA741 Electrical Characteristics: $V_{CC} = \pm 15$ V, $T_A = 25°C$

Characteristic	*MIN*	*TYP*	*MAX*	*Unit*
V_{IO} Input offset voltage		1	6	mV
I_{IO} Input offset current		20	200	nA
I_{IB} Input bias current		80	500	nA
V_{ICR} Common-mode input voltage range	±12	±13		V
V_{OM} Maximum peak output voltage swing	±12	±14		V
A_{VD} Large-signal differential voltage amplification	20	200		V/mV
r_i Input resistance	0.3	2		MΩ
r_o Output resistance		75		Ω
C_i Input capacitance		1.4		pF
CMRR Common-mode rejection ratio	70	90		dB
I_{CC} Supply current		1.7	2.8	mA
P_D Total power dissipation		50	85	mW

Note: These ratings are for specific circuit conditions, and they often include minimum, maximum and typical values.

CMRR

One rating that is unique to op-amps is CMRR or common-mode rejection ratio.

Because the op-amp has two inputs that are opposite in phase (inverting input and the non-inverting input) any signal that is common to both inputs will be cancelled.

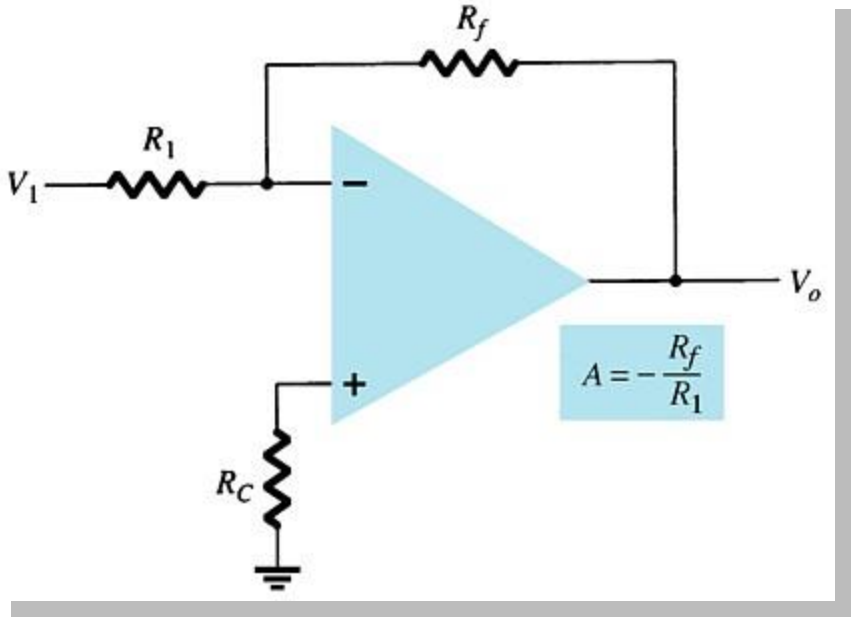
Op-amp CMRR is a measure of the ability to cancel out common-mode signals.

Op-Amp Applications

Constant-gain multiplier
Voltage summing
Voltage buffer
Controlled sources
Instrumentation circuits
Active filters

Constant-Gain Amplifier

Inverting Version



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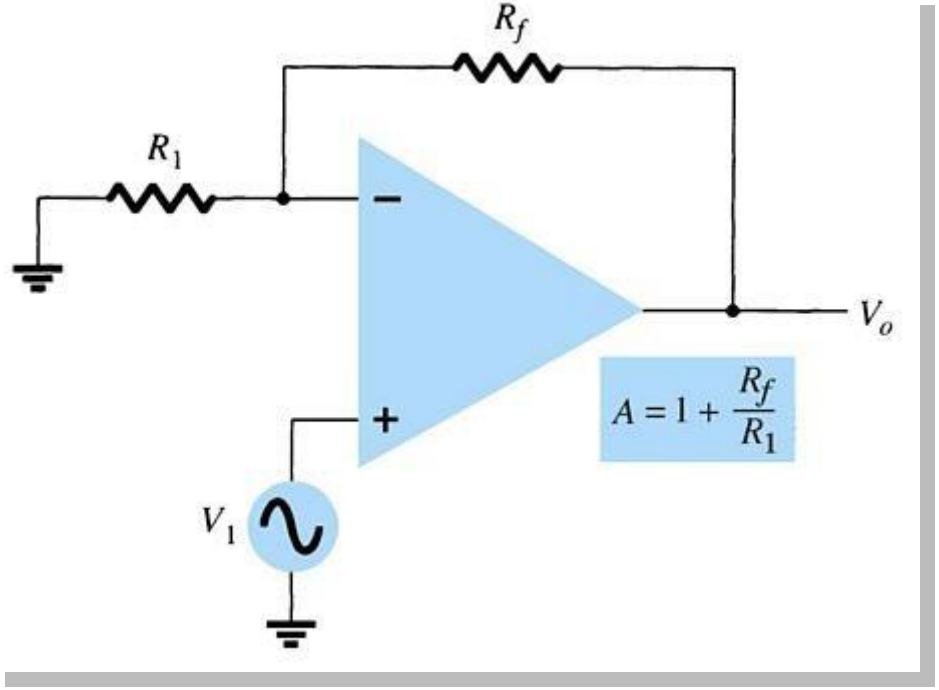
Constant-Gain Amplifier

Noninverting Version



Multiple-Stage Gains

The total gain (3-stages) is given by:

$$A = A_1 A_2 A_3$$

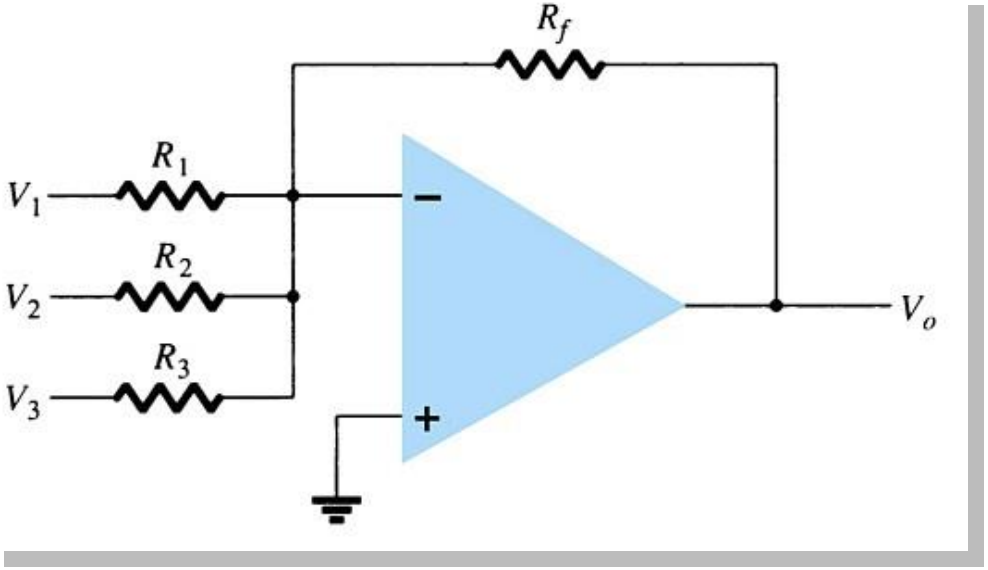
or

$$A = \left(1 + \frac{R_f}{R_1}\right)\left(-\frac{R_f}{R2}\right)\left(-\frac{R_f}{R3}\right)$$

Voltage Summing

The output is the sum of individual signals times the gain:

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$



[Formula 14.3]

Week - 15

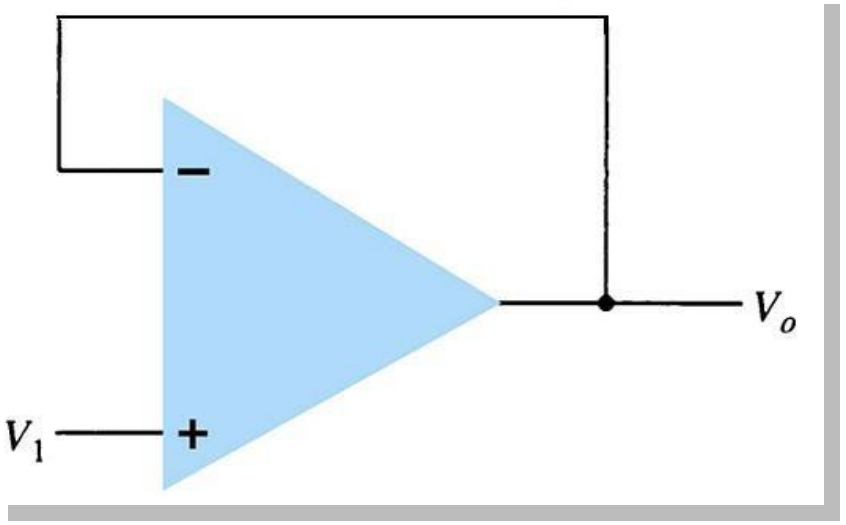
Voltage Buffer

Any amplifier with no gain or loss is called a unity gain amplifier.

The advantages of using a unity gain amplifier:

- **Very high input impedance**
- **Very low output impedance**

Realistically these circuits are designed using equal resistors ($R_1 = R_f$) to avoid problems with offset voltages.



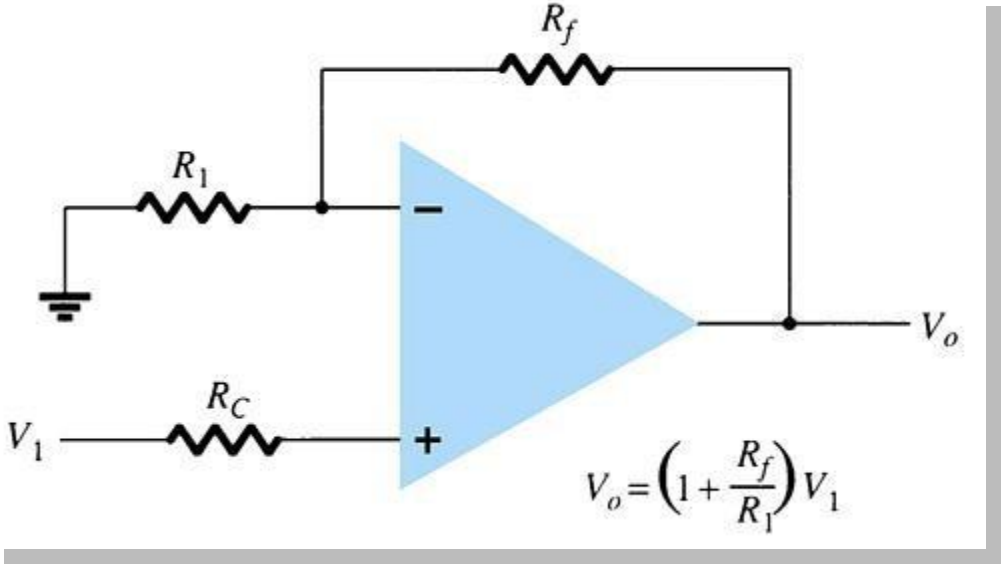
Controlled Sources

Voltage-controlled voltage source
Voltage-controlled current source
Current-controlled voltage source
Current-controlled current source

Voltage-Controlled Voltage Source

The output voltage is the gain times the input voltage. What makes an op-amp different from other amplifiers is its impedance characteristics and gain calculations that depend solely on external resistors.

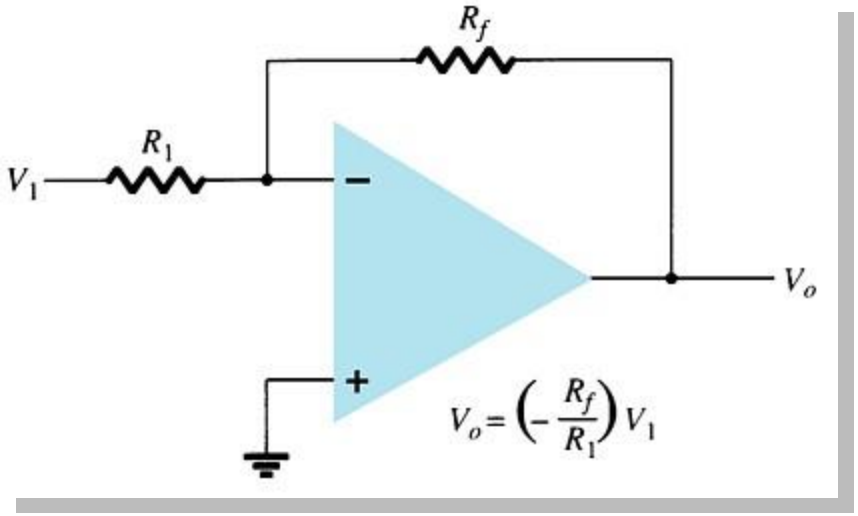
Noninverting Amplifier Version



Voltage-Controlled Voltage Source

The output voltage is the gain times the input voltage. What makes an op-amp different from other amplifiers is its impedance characteristics and gain calculations that depend solely on external resistors.

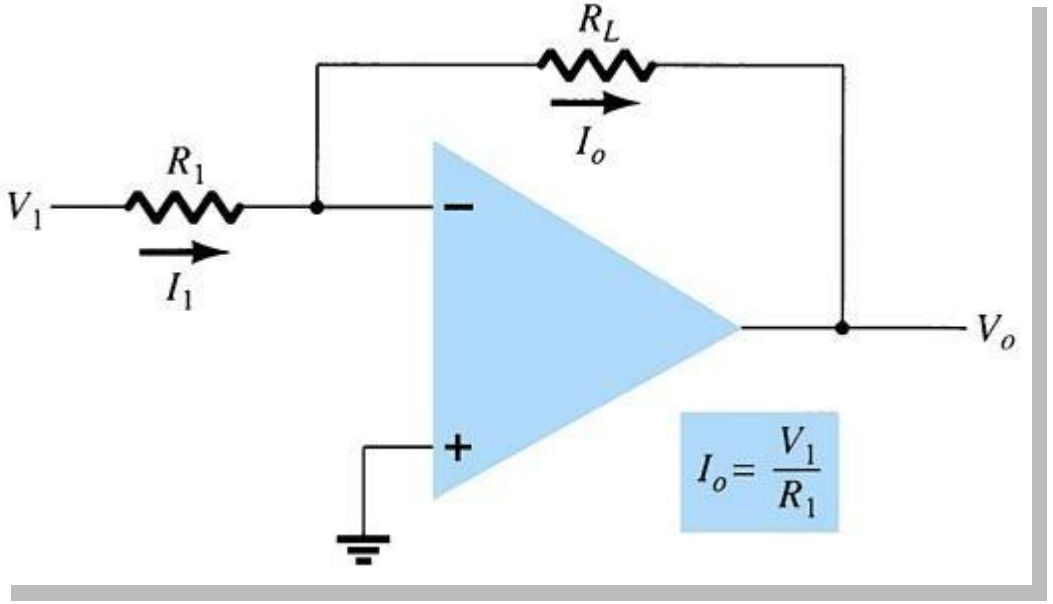
Inverting Amplifier Version



Voltage-Controlled Current Source

The output current is:

$$\mathbf{I_o = \frac{V_1}{R_1} = kV_1}$$



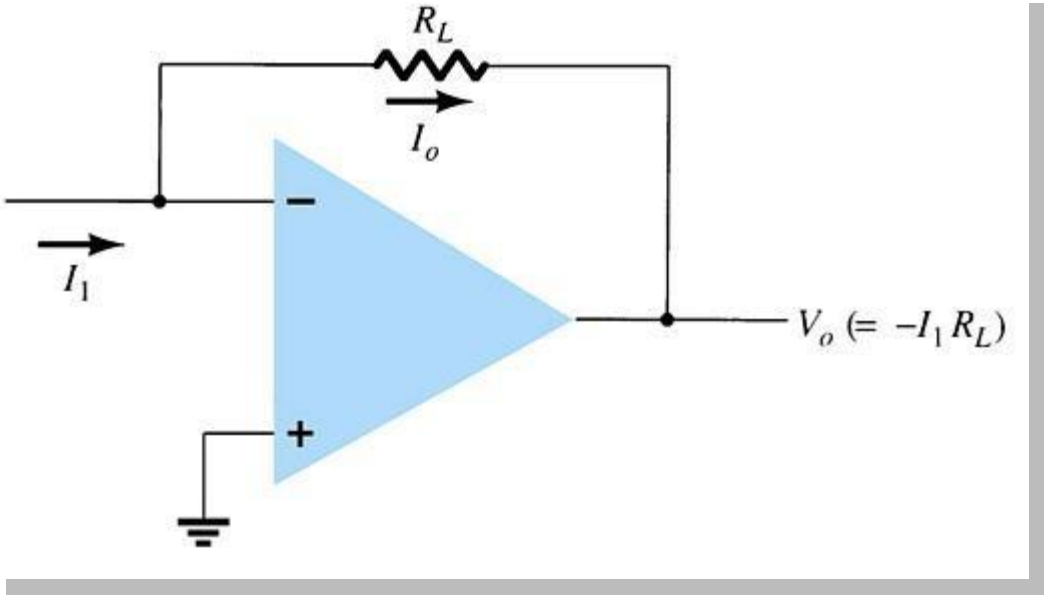
Current-Controlled Voltage Source

This is simply another way of applying the op-amp operation. Whether the input is a current determined by V_{in}/R_1 or as I_1:

$$V_{out} = \frac{-R_f}{R_1} V_{in}$$

or

$$V_{out} = -I_1 R_L$$



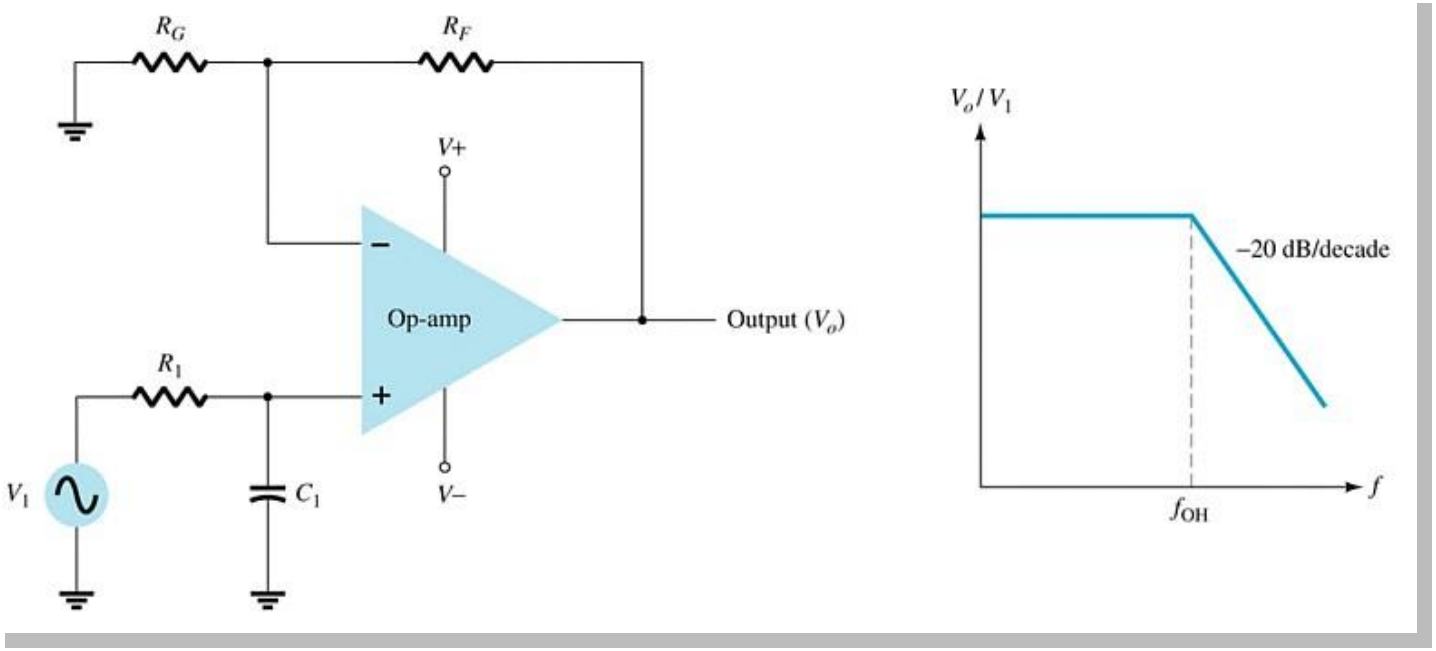
Active Filters

Adding capacitors to op-amp circuits provides external control of the cutoff frequencies. The op-amp active filter provides controllable cutoff frequencies and controllable gain.

- **Low-pass filter**
- **High-pass filter**
- **Bandpass filter**

Week - 16

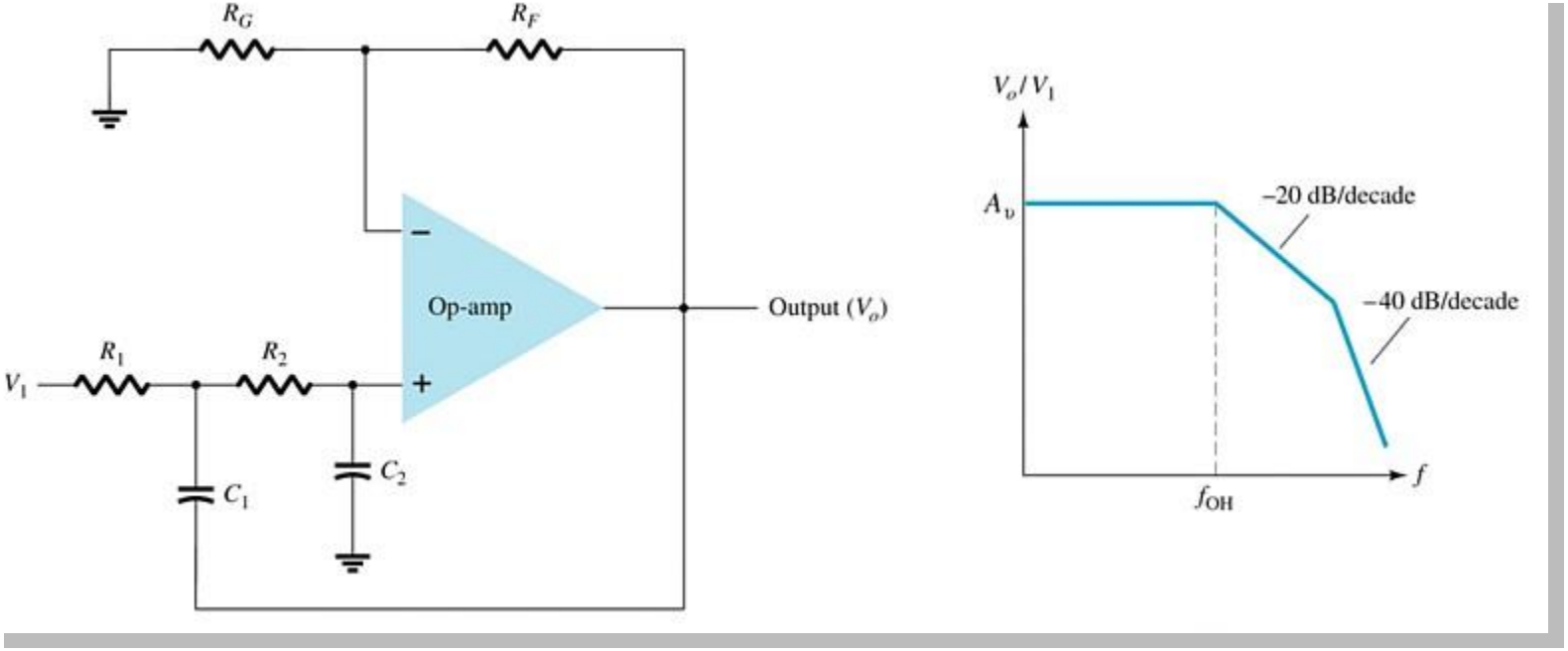
Low-Pass Filter—First-Order



The upper cutoff frequency and voltage gain are given by:

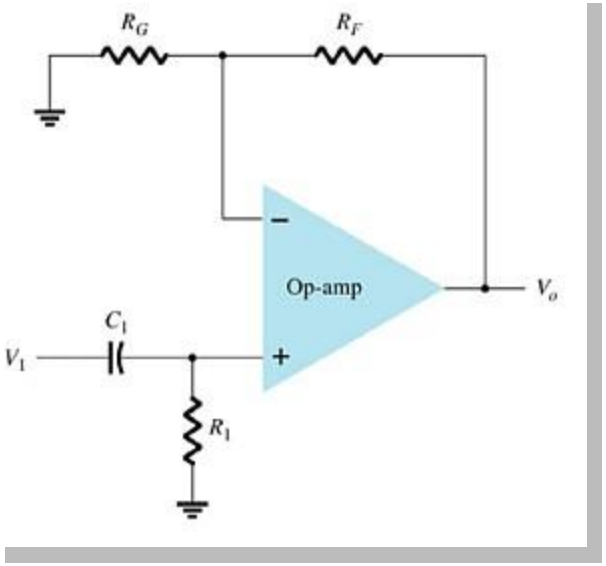
$$f_{OH} = \frac{1}{2\pi R_1 C_1} \qquad A_v = 1 + \frac{R_f}{R_1}$$

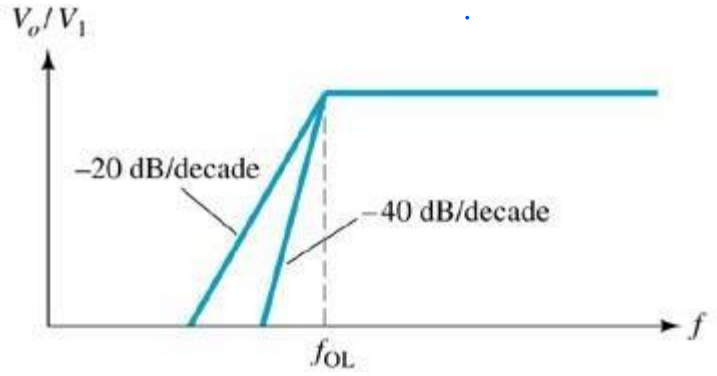
Low-Pass Filter—Second-Order



The roll-off can be made steeper by adding more RC networks.

High-Pass Filter



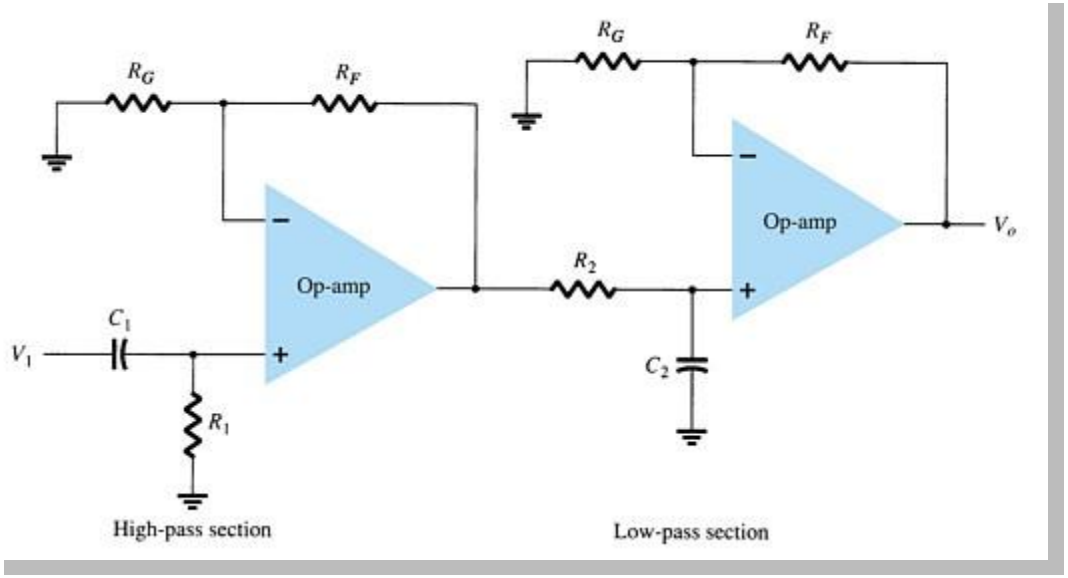


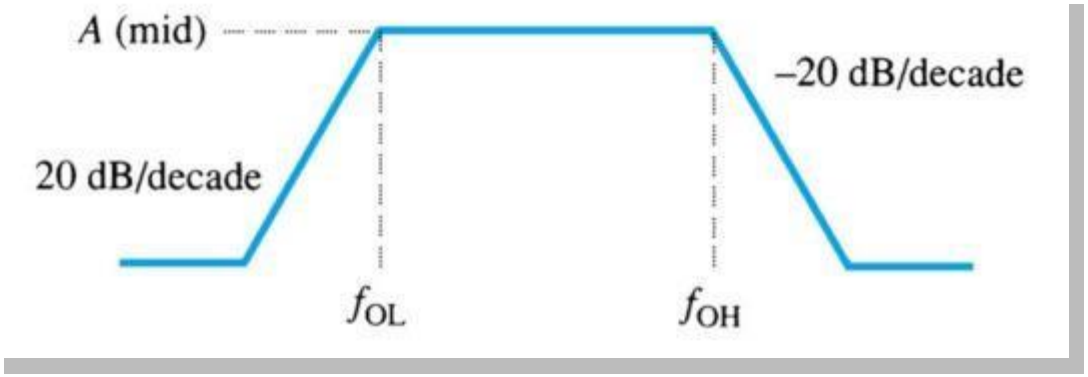
The cutoff frequency is determined by:

$$f_{OL} = \frac{1}{2\pi R_1 C_1}$$

Bandpass Filter

There are two cutoff frequencies: upper and lower. They can be calculated using the same low-pass cutoff and high-pass cutoff frequency formulas in the appropriate sections.





Week - 17

- Mathematical Problem Solving (Will be Discussed in Class)
- Presentation on Selected Topics

Thank You!